IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent application of:

Applicant(s): Paul A. Kohl et al.
Serial No: 09/717,567
Filing Date: November 21, 2000
Title: FABRICATION OF A SEMICONDUCTOR DEVICE WITH AIR GAPS FOR ULTRA-LOW CAPACITANCE INTERCONNECTIONS

Examiner: James M. Mitchell
Art Unit: 2827

Docket No. PRMSP0217USA

DECLARATION UNDER 37 C.F.R. § 1.132

Sir:

I, Bernard Berman of 1220 W. 6th Street, Suite 700, Cleveland, Ohio 44113, hereby declare as follows:

1. I am Patent Counsel at Promerus LLC, located at 9921 Brecksville Road, Brecksville, Ohio 44141. I hold Bachelors and Masters Degrees in Chemistry from Post College of Long Island University and Rutgers, the State University of New Jersey, respectively. In addition, I hold a Juris Doctorate degree from Arizona State University.

2. While I am one of the attorneys of record of the above invention, I have personal knowledge of and considerable experience with the subject matter of the patent application to which this Declaration is addressed.

3. Prior to joining Promerus, I worked for the Semiconductor Sector of Motorola, Inc., located in the Phoenix, AZ metropolitan area, for more than 19 (nineteen) years. During this time, I held various positions directed to research and development of semiconductor processing, and direct engineering support of the manufacture of integrated circuit devices. These positions included both the Process Engineering and Device Engineering

Manager of a wafer fabrication facility internally known as BiPolar II in Mesa, AZ and Engineering and Assistant Fab Manager of a wafer fabrication facility internally known as MOS 6, also in Mesa, AZ. These positions required detailed and highly technical knowledge of all processes and materials employed in the conversion of a bare, single crystal silicon wafer into an array of integrated circuits formed thereon.

4. The BiPolar logic and memory devices manufactured in the aforementioned BiPolar II facility were among the first devices manufactured by Motorola having multiple levels of metallization and during the years from 1980 to 1984, I was responsible for the initial development of APCVD (Atmospheric Pressure Chemical Vapor Deposition) and PECVD (Plasma Enhanced CVD) processes used to form an interlayer dielectric layer for providing electrical isolation between the metal layers formed over the wafers.

5. During the development of these processes, various deposition conditions and parameters were evaluated using test substrates having a broad range of structure height, width and spacing from adjacent structures. Routinely, the results of our deposition trials were evaluated using Scanning Electron Microscopy (SEM) to visualize a cross-section of test structures. I observed that in all cases where test structures had a cross-sectional profile that was close to perpendicular, the dielectric coating was formed in a non-uniform manner that was referred to as "bread-loafing" (see, Fig. 1 in Attachment A). This non-uniform coating profile resulted in the formation of gaps between those adjacent structures where the bread-loafing on such structures closed the space there between to any further deposition. These gaps were called "key-hole" or "tear-drop" defects because of their shape as is shown in Fig. 2 of Attachment A.

6. At the time of my development work, the minimum feature size of the BiPolar devices I manufactured were at least an order of magnitude larger then

current state of the art devices. RC time constant and cross-talk issues were unknown and as a result, the aforementioned gaps were viewed as defects and considerable effort was expended to eliminate them. Extensive testing of deposition conditions, chemicals, and equipment was performed and in all cases the formation of a key-hole/tear-drop defect was always found.

7. I have carefully reviewed the newly cited art and the figure that depicts a uniformly shaped gap between adjacent conductive traces having near perpendicular profiles. Based upon the art's description of the process employed for dielectric deposition, I can state that there was no deposition method known at the time such art was created that could have formed such a structure. Furthermore, I can state that even with the advances in deposition technology that have become known today, it is still impossible for such a uniformly shaped structure to be formed by deposition. Still further I can state that these statements are facts widely known to those of ordinary skill in the art and such knowledge is demonstrated by and through the several recent publications provided in Attachment B at the top of page 15 and in figures 2, 4 and 5 of Attachment C.

8. Finally I state, as a person of skill in this art, that any other ordinarily skilled person reading the cited art would recognize that the gaps shown in the principal figure of the art could not be made by the process described therein and therefore such art does not and can not anticipate or make obvious the uniformly shaped air-gaps of the instant application.

Date: Aug 22, 2007

Bernard Berman, Reg. No. 37,279

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Integration of SiOC air gaps in copper interconnects

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Abstract

The formation of air gaps by means of a non-conformal chemical vapor deposition (CVD) on patterned wafers was successfully demonstrated using SiOC (K=2.9) as inter-level metal dielectric. This paper presents the results on physical characterization and electrical performance evaluation of integrated SiOC air gaps in a three-metal level Cu/SiOC interconnect module. The influence of the air gaps shape on parasitic coupling capacitance between copper lines was also discussed in accordance with mask design rules and processing steps.

Keywords: Air gap; Ultra-low K; PECVD dielectrics; Copper interconnect; Dual damascene architecture

1. Introduction

Due to the constant decrease of dimensions in interconnections related to integration density for sub-90-nm CMOS technologies, coupling capacitances between neighbouring copper lines become the limiting factor for integrated circuit performance as they increase propagation time delay and cross-talk. After several ultra-low K dielectric generations, the International Technology Roadmap for Semiconductors [1] recommends the use of air cavities in-between copper lines, hereafter referred to as air-gaps, in order to decrease the effective dielectric constant beyond 2.5. One approach to achieve this goal is the formation of air gaps using a non-conformal CVD deposition on patterned wafers [2,3]. This paper presents data from several physical and electrical characterization methods obtained for air gaps built in bulk SiOC using this technique. The results will be discussed in terms of performance in relation with critical processing steps.

2. Experimental

SiOC air-gaps were incorporated at metal 2 in a three-metal level SiOC/Cu interconnect stack using 120 nm generation design rule and 248 nm lithography technique. Fig. 1 illustrates the technological sequence used for air gap integration: (i) once a Cu metal interconnect level is completed in SiOC at metal 2 using the metallization process conditions previously detailed in Refs. [4–6], (ii) an additional lithography step is introduced to define air gap trenches in-between copper lines and the as-defined trenches are then etched using a dry plasma etching process. (iii) Then 40 nm of SiC (K=4.5) and 600 nm of SiOC (K=2.9) inter-metal dielectric (IMD)

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Attachment A

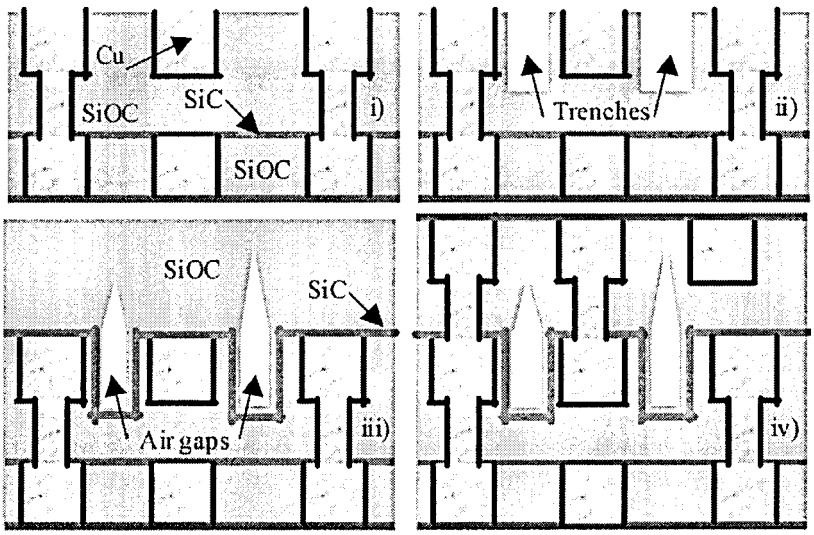

Fig. 1. Schematic representation of integration process flow for the fabrication of SiOC air gaps between Cu interconnects: (i) SiOC-Cu integration at metal 2, (ii) additional lithography and trenches etching, (iii) air gaps formation inside trenches after sequential deposition of a SiC liner and bulk SiOC, and (iv) via-first dual damascene process to complete the integration.

are successively deposited to fabricate the SiOC air gaps. (iv) After that, a chemical mechanical polishing (CMP) process was used to planarize the dielectric surface and the interconnect stack was completed for the metal 3 level using a via-first dual-damascene architecture.

The air gap trenches were controlled in width and height (see Fig. 2a–c) so that the aspect ratio, defined as the ratio between the height and the width of the trenches, was above 1 as required for well-shaped cavity creation [7–9]. To achieve these requirements and precisely control air gap morphology (i.e., closure point height, width, volume, etc.), the trench width on the specific air gap mask was set to 0.2 μm (Fig. 2b). Using this approach, it is possible to take advantage of a constant aspect ratio of the air gap trenches making the air gap morphology dependent only on the step coverage properties of the CVD process (Fig. 2c). Reference SiOC/Cu wafers without air gaps were processed in parallel for electrical performance (leakage current and parasitic coupling capacitance measurement between Cu lines at metal 2 level) evaluation of the SiOC air gaps for shifted and stacked comb/serpentine structures with 2 μm wide Cu lines and a metal spacing ranging from 0.2 to 0.4 μm.

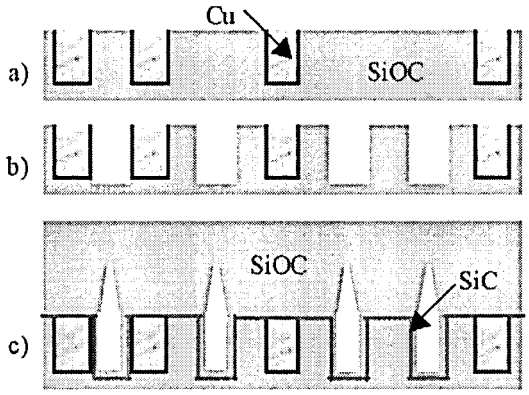

Fig. 2. Schematic representation of SiOC air gaps' integration strategy detailed in the text used in this study to evaluate SiOC air gap performances in Cu interconnects. (a) one metal level SiOC/Cu interconnect stack; (b) SiOC air gap trenches formation; (c) SiOC air gaps fabrication.

To complete our understanding of the air gap formation process, a second set of interconnect structures was fabricated at metal 1 level. The fabrication of SiOC air gaps was investigated by screening the non-conformal CVD deposition time for bulk SiOC. At the same time, to study the influence of an intermediate USG layer on air gap morphology, 200 nm of SiOC and 80 nm of SiO_2

using TEOS as precursors were successively deposited to form and close the air gaps. Then, the IMD was finally encapsulated after 300 nm of SiOC were deposited above the bi-layer.

3. Results and discussion

3.1. Morphological characterization

Non-conformal CVD air gap integration issues are mainly related to the shape control of the cavities. More especially, it is necessary to make sure that misalignment between lithography of line and via levels and upper level lines etching do not introduce any breakthrough into the air gaps. Indeed some metal intrusion in the cavities would be fatal for electrical performances and for interconnects reliability.

3.1.1. Trenches patterning

In order to overcome the previous mentioned issues, the width of the trenches was set to 0.2 μm that is the minimum metal spacing available on the test vehicle. Moreover, the depth of the trenches must also be correctly chosen, as some dielectric will be deposited at the bottom and the sidewalls of the trenches during SiC and SiOC deposition. As a consequence, trenches must be etched deep enough so that air gaps are as wide as possible all along the metal lines. Moreover, another concern is the uniformity control during etching and IMD deposition steps to prevent some air gap opening during the integration. Indeed, any etch or deposition discrepancy between the edge and the centre of the wafer would directly, respectively, impact (i) the aspect ratio of the air gap trenches and as a matter of fact the closure point height of the air gaps in the IMD and (ii) the total IMD thickness.

3.1.2. Air gap formation by CVD process

After air gap trenches formation inside SiOC in-between Cu metal lines, a thin SiC dielectric liner was first deposited in order to improve electrical performance and reliability as previously demonstrated for SiO_2 air gaps in combination with SiN ($K=7$) as liner [4]. However, the step coverage properties of the SiC liner will also impact the further SiOC deposition and thus, the final air gap shape.

To summarize, air gaps must be as narrow as possible above the copper lines to prevent via-misalignment, while at the same time, the cavity width must be large enough to obtain the best low-K performance [2]. At the same time, the closure of the air gaps must occur low enough inside via level to prevent metal intrusion inside the cavities when metal lines are integrated directly above air gaps. It was observed after complete integration (Fig. 3) that the SiOC air gaps were 100 nm wide with closure point height situated approximately at 250 nm above the copper lines. This mean value is high considering that the IMD thickness at via level was fixed at 300 nm high in our integration architecture.

Non-conformal CVD air gaps integration faces surface uniformity issues after complete dielectric deposition. In a previous study, flat dielectric surface were obtained using pure or sequential undoped silicon glass (USG) deposition steps [4–6]. Here, a surface roughness of 50 nm was measured after SiOC deposition (Fig. 4). This roughness, due to step coverage properties of SiOC of our deposition process, is not acceptable for further process integration. Therefore, an additional planarization using dielectric CMP was introduced and no mechanical breakthrough of the air gaps during this step was observed demonstrating the good mechanical strength of the SiOC air gaps during this process step.

In order to decrease the height of the cavities, the influence of the incorporation of an intermediate dielectric TEOS-based USG (USGT) layer inside the

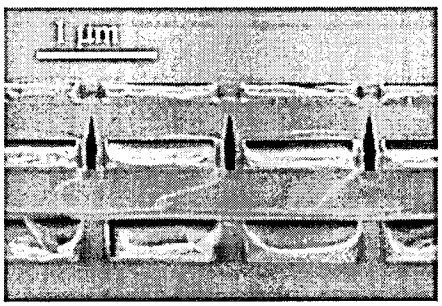

Fig. 3. SEM cross-section of comb structures perpendicularly stacked from metal 1 to metal 3 levels with SiOC air gaps at metal 2.

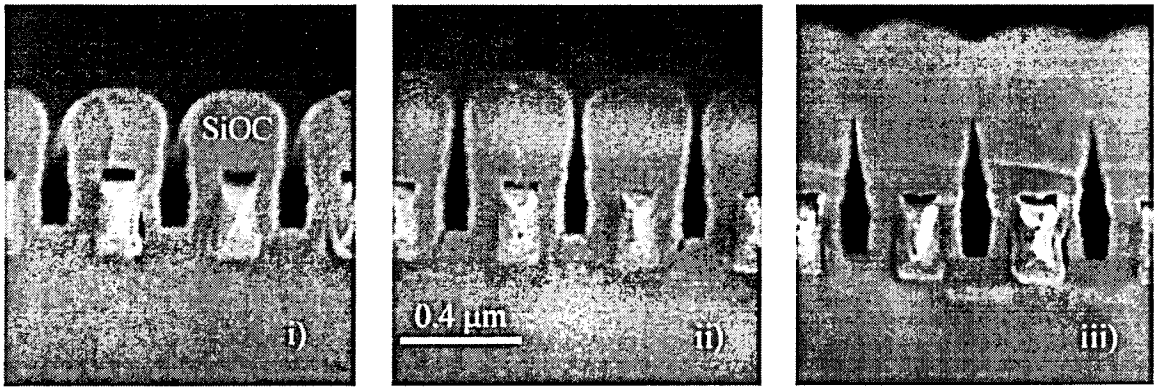

Fig. 4. SiOC air gaps growth formation study using non-conformal CVD deposition properties in pattern wafers (pitch (=metal width+metal space)=0.4 µm) as a function of SiOC thickness. SEM cross-section images of the patterning structures were taken after the successive deposition of a 40-nm thick SiC liner and of (i) 200, (ii) 300, and (iii) 600 nm of SiOC.

SiOC stack was studied. TEOS was preferred to silane (SiH_4) as a precursor for USG deposition because of its higher step coverage [6]. From growth kinetics results for pure SiOC air gaps previously illustrated in Fig. 4, an intermediate 80 nm thick USGT layer was incorporated inside the SiOC IMD layer after 200 nm of SiOC were first deposited. As a consequence, a significant lowering by 20% to 200 nm of the closure point height was observed in these conditions (Fig. 5). Therefore, this approach could be a promising solution to overcome air gap opening during the whole integration. However, at the same time, the cavity volume between the copper lines was highly reduced, due to some USG deposition on the cavities sidewalls, thus increasing the effective dielectric constant of the IMD between the lines. Moreover, the surface planarity was not enough improved, thus making dielectric CMP still necessary before complete realization of the interconnect stack.

3.2. Electrical results

The evolution of the intra-metal level parasitic coupling capacitance between combs and serpentines with or without SiOC air gaps at metal 2 as a function of the metal spacing is presented in Fig. 6. For the narrowest pitch, where air gaps are the most useful for delay and crosstalk improvement, the best performance was obtained as a decrease by 20% of M2–M2 coupling capacitances after introduction of the cavities was observed. However, it is also interesting to note that as air gap width was fixed, the influence of SiOC air gap on electrical per-

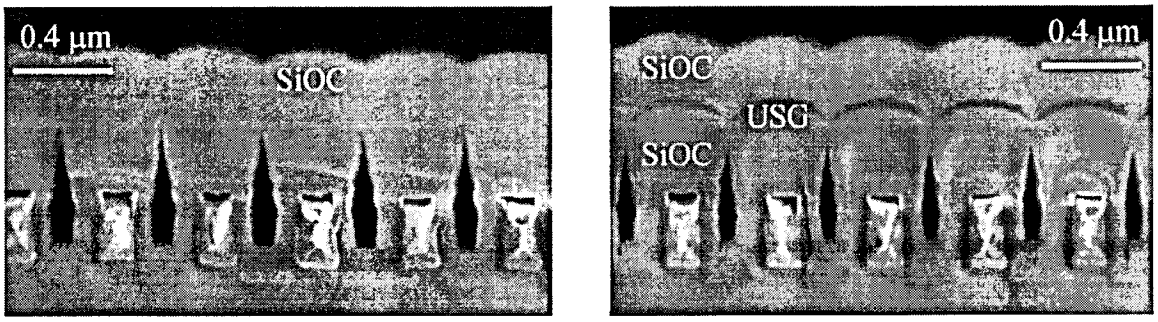

Fig. 5. SEM cross-section images of 'SiOC' air gaps fabricated in pure SiOC (left) or using a three-step process in which 200 nm of SiOC, 80 nm of USGT (TEOS-based USG, and finally 300 nm of SiOC are successively deposited (in both cases, a 40-nm thick SiC liner is first deposited above Cu lines).

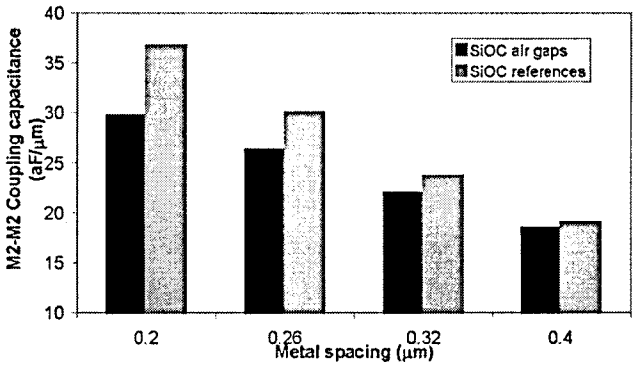

Fig. 6. Measured M2–M2 parasitic coupling capacitance for SiOC air gaps and SiOC reference wafers for comb/serpentine shifted structures and 2 µm width Cu lines.

formance decreases when metal spacing increases as expected, until being even negligible for 0.4 µm wide metal space. The introduction of air gaps had no incidence on the leakage current values measured for these structures.

From electrical simulation of the interconnect stack of these structures, the lowest extracted effective dielectric constant between metal 2 lines obtained using SiOC air gaps was 2.1. Noticeable SiOC deposition on the sidewalls of the trenches as well as fringe coupling capacitances characteristics of these air gaps could explain that this value is similar to that obtained for SiO_2 air gaps using a SiN liner [4].

In some cases, the measured M2–M2 coupling capacitances highly varied when metal 1 and metal 3 were grounded or let floating. This phenomenon is probably due to some metal intrusion in the cavities as some breakthrough of the air gaps was predicted from the closure height variations on the wafer surface as previously described. However, no degradation of the leakage current performances was observed for these non-reliable electrical structures (not shown).

The influence of a sequential deposition treatment using successively SiOC and USGT on the M2–M3 coupling capacitance was also investigated. The simulated interconnect stack presented in Fig. 7 is characterized by air gaps fabricated in pure SiOC and the IMD (SiOC+USG) thickness was set to 300 nm. The simulations showed a capacitance increase lower than 10% when the USG layer is thinner than 100 nm. This result stays still far under the capacitance value of full USG air gaps keeping the same geometry for the interconnect stack. Once the step coverage of both SiOC and USG deposition process above trenches optimised, sequential SiOC/USG/

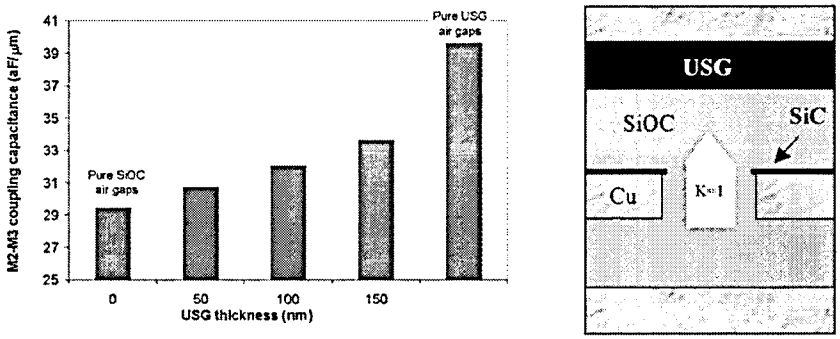

Fig. 7. (Left) Simulated M2–M3 coupling capacitance as a function of the USG thickness in a SiOC stack (the total IMD thickness (SiOC+USG) is 300 nm) in a three-metal level interconnect stack (right) that slightly differs from integrated interconnect test structures.

SiOC deposition steps could be a good compromise to achieve the best low-K performance (i.e., a high gap volume) and improve integration reliability of the air gaps (i.e., a low tip-end height control above the metal lines).

4. Conclusion

Integration of SiOC air gaps using a non-conformal CVD deposition on pattern wafers was successfully demonstrated for the first time. In particular, the morphology and the electrical performances of these air gaps were investigated and their dependence with mask design rules and processing steps discussed. Finally, an intermediate USG layer was showed to significantly lower the air gap closure point inside the IMD level in order to successfully prevent via-misalignment issues. These results open interesting perspective to achieve good reliability of air gaps with ultra low-K performances.

Acknowledgements

The authors would like to thank S. Courtas from characterization group for her support for SiOC air gaps observation using FIB/MEB techniques.

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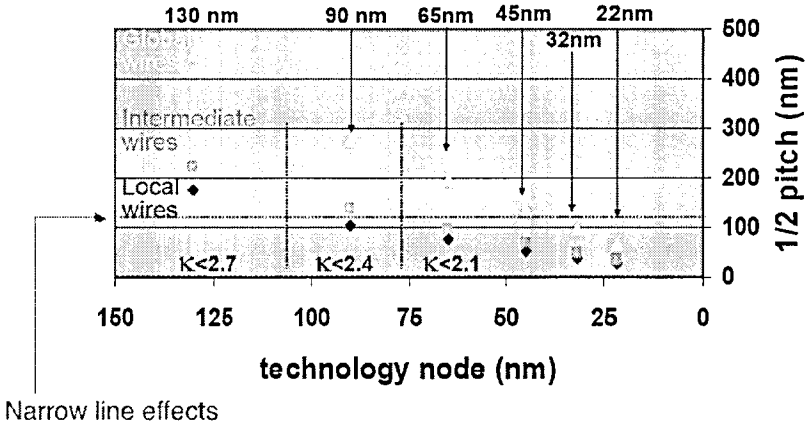
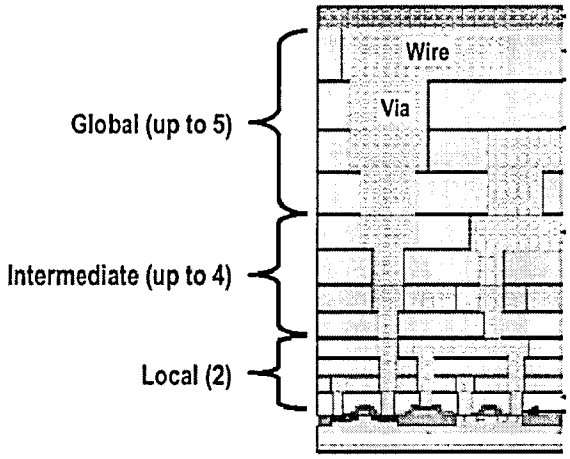
Deposition & Planarization

Scaling of interconnects requires more metal layers with reduced interconnect pitch. The height of metal has to be increased. The increased aspect ratio between the metal lines will increase dramatically the problem of step coverage.





The interconnect topography can cause problems in step coverage and lithography.

Depth of Focus in Lithography

From optics:

$$F_{number} = \frac{f}{D} = \frac{\text{focal length of lens}}{\text{diameter of lens}}$$

$$\text{Resolution} = 1.22\lambda F_{number}$$

$$\text{Depth of field} = \pm 2\lambda F_{number}^2$$

Example:
We need to resolve 0.1 μm lines and spaces
If λ = 180 nm for the light source, we need F_{number}=0.45 to resolve 0.1 μm features

Depth of field = $\pm$ 0.07 μm

Resolution can be increased but the depth of field will decrease.

Gate stack for a 0.1 μm MOS transistor is shown in Fig. 2. It will be difficult to define features simultaneously at the top and the bottom surfaces of this type of structure.

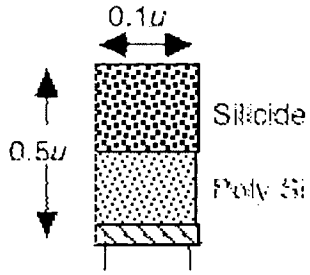
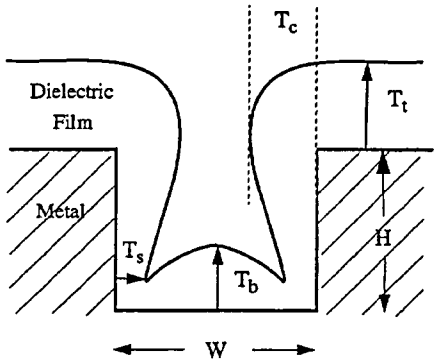


Fig. 2

Step Coverage



$$\text{Aspect Ratio} = \frac{H}{W}$$

$$\text{bottom step coverage} = \frac{T_b}{T_t}$$

$$\text{side step coverage} = \frac{T_s}{T_t}$$

$$\text{cusping} = \frac{T_c - T_s}{T_s}$$

Fig. 2 Step coverage definitions. Poor step coverage results from different deposition rates in different parts of a nicrostructure.

The profile of the thin films deposited by any of the CVD or PVD techniques depend upon:

1. Equipment configuration
2. Deposition method (LPCVD, PECVD, PVD)
3. Reaction chemistry
4. Reactant transport mechanism

Deposition Techniques

Chemical vapor deposition (CVD): Deposition occurs as a byproduct of a chemical reaction in vapor phase.

Physical vapor deposition (PVD): Deposition occurs as a byproduct of a physical process, such as, evaporation from a source followed by condensation on another surface.

Chemical Vapor Deposition Systems

Various chemical vapor deposition (CVD) techniques are commonly used for semiconductor processing. Deposition temperatures vary from 100°C to 1000°C, and pressure ranges from atmospheric to the milliTorr regime. The energy for the reaction can be thermal, photochemical or electrical (for plasma processes). For each of these techniques there is a wide range of reactor configurations which have been used.

Atmospheric Pressure Chemical Vapor Deposition (APCVD)

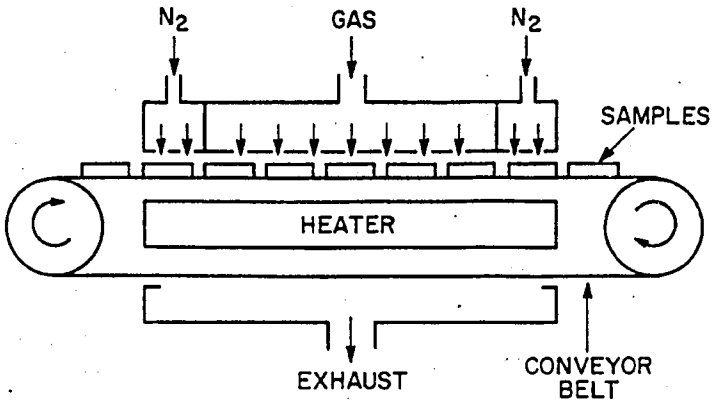


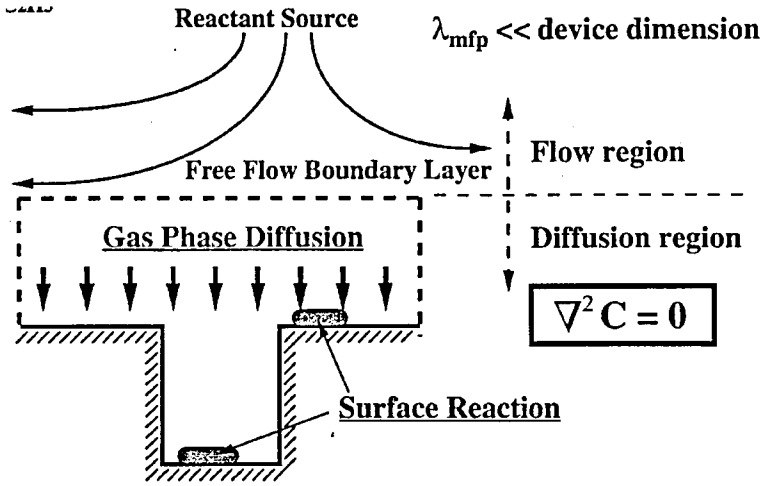
Fig. 5. Continuous Flow Atmospheric Pressure Reactor

In the early days of semiconductor processing atmospheric pressure reactors were used to deposit silicon and dielectric films. The advantage of deposition at atmospheric pressure is the simplicity of the reactor design and that high deposition rates are obtained. Although several different reactor geometries were used, the operating principle is the same in all these reactors. The wafers are put on a hot susceptor and reactant gases flow over the susceptor. The susceptor is heated by using high-intensity lamps, radio frequency induction, or dc electric current (resistive) heating. These atmospheric pressure reactors have low throughput, require excessive wafer handling during wafer loading and unloading and have poor thickness uniformity (>- 10%) across the wafer.

To overcome some of these disadvantages, continuous throughput atmospheric pressure reactors were developed. In these reactors the wafers are carried through the reactor on a conveyor belt and are heated by convection. Also, there is a more uniform flow of the reactant gases across the wafer surface. These reactors have high throughput, good uniformity and the ability to handle large diameter wafers. The main disadvantages of this type of reactor are that they required frequent cleaning and that particles formed on the reactant dispenser head wind up on the wafers which impaired process yield and device reliability.

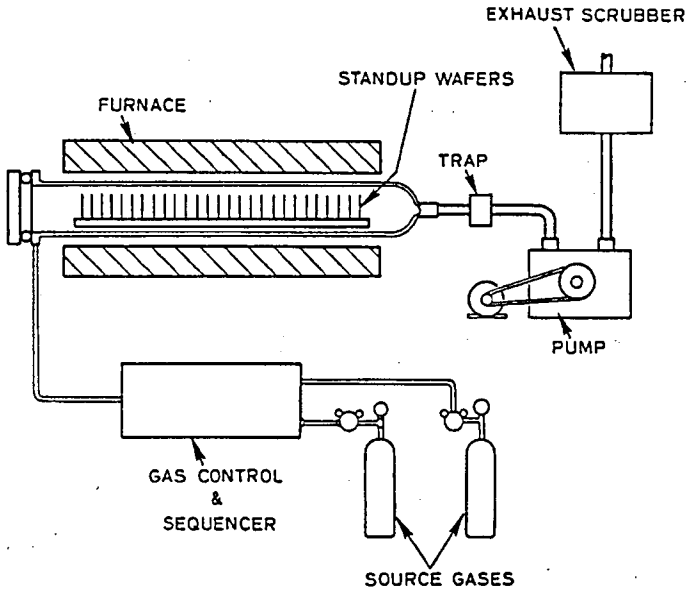
Transport of reactants to the surface at atmospheric pressure

Mean free path in the gas phase is much smaller than the dimensions of features on a wafer. Gas-gas collisions control the transport.



Mean free path in the gas phase is much larger than the dimensions of features on a wafer. Surface collisions and re-emission control the transport.

Low Pressure Chemical Vapor Deposition (LPCVD) Reactors



$$Dep.rate = \frac{kh}{k+h} \cdot \frac{N_g}{n}$$

$$where\ the\ mass\ transfer\ coefficient\ h \propto Diffusivity \propto \frac{1}{pressure}$$

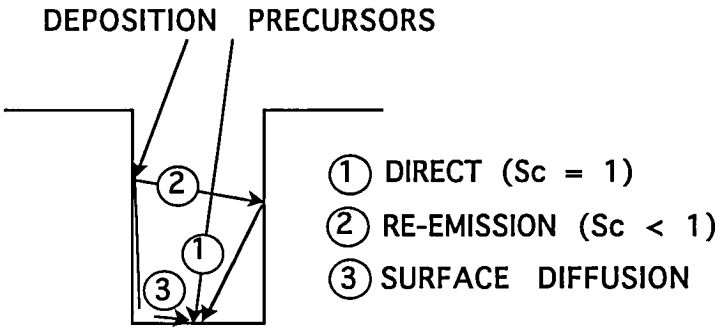
Where k is the surface reaction rate constant and N_g/n gives the concentration of the depositing species.

Low pressure chemical vapor deposition reactors were developed to overcome the disadvantages of the high pressure systems discussed above. One of the difficulties in the cold wall systems (where only the susceptor holding the wafer is heated) described above is maintaining a uniform temperature across the wafer surface. This can be overcome by putting the entire reaction chamber in a furnace maintained at a uniform temperature as in the case of standard resistance heated hot wall tubular furnaces. A large number of wafers can be stacked closely in these furnaces and good uniformity across the wafer and wafer to wafer film thickness can be achieved if they are operated at very low pressures and in the surface reaction limited regime. The transport of the reactant gases to the wafer surface in these reactors is by gas phase diffusion. At very low pressures the diffusion coefficients of the gas phase species is very large and if the process is surface reaction limited, there is an approximately uniform distribution of the reactive gas phase species throughout the reaction chamber, which results in a uniform fllm deposition.

Figure above gives the schematics of a hot-wall, low pressure chemical vapor deposition reactor used to deposit polycrystalline silicon, silicon dioxide and silicon nitride. The reactor consists of a quartz tube heated by a resistance heated furnace to maintain a uniform temperature along the reactor. Gases are introduced in one end and pumped out from the other end of the reactor. The operating pressures range from 0.25 Torr to 2 Torr and temperatures range from 300 to 900°C, and gas flow rates range from 100 to 1000 sccm. A large number of wafers (~ 100) are stacked vertically, perpendicular to the gas flow, in a quartz holder. The inlet gases may undergo homogeneous gas phase reactions to produce the deposition precursors which are transported to the wafer surface by gas-phase diffusion. Excellent film uniformities (±5%) are obtained in these reactors. Although these reactors have lower deposition rates, it is found that this is more than compensated for by the high wafer capacity.

With increasing wafer size, the film uniformity in the low pressure batch reactors tends to decrease. It should be mentioned that the future trend is towards single wafer processing systems instead of the batch system described above. This is because of the increasing wafer sizes (8" or higher), and the development in technology to achieve better film uniformity and higher deposition rates in modern single wafer reactors.

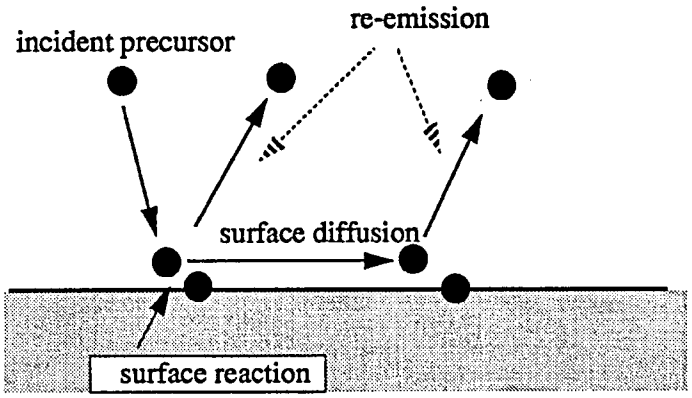
Transport of reactants to the surface at low pressures



In most applications surface diffusion has been found to be negligible.

Sticking Coefficient

S_C - Reactive sticking coefficient is the probability of an incident deposition precursor



$$S_c = \frac{\Gamma_{incident} - \Gamma_{re-emission}}{\Gamma_{incident}} = \frac{\Gamma_{reaction}}{\Gamma_{incident}}$$

Typical deposition pressures

Low pressure CVD (LPCVD) ~ 0.5 Torr
PECVD 0.5 m Torr - 1 Torr
Sputtering 1 - 20 x 10^{-3} Torr

Mean Free Path $\lambda_m = \frac{1}{260P}$ cm where P is the pressure

Pressure(torr)	760	1	0.1	.01	0.001
λ_m (Cm)	6.26×10^{-6}	4.5×10^{-3}	4.5×10^{-2}	0.45	4.5

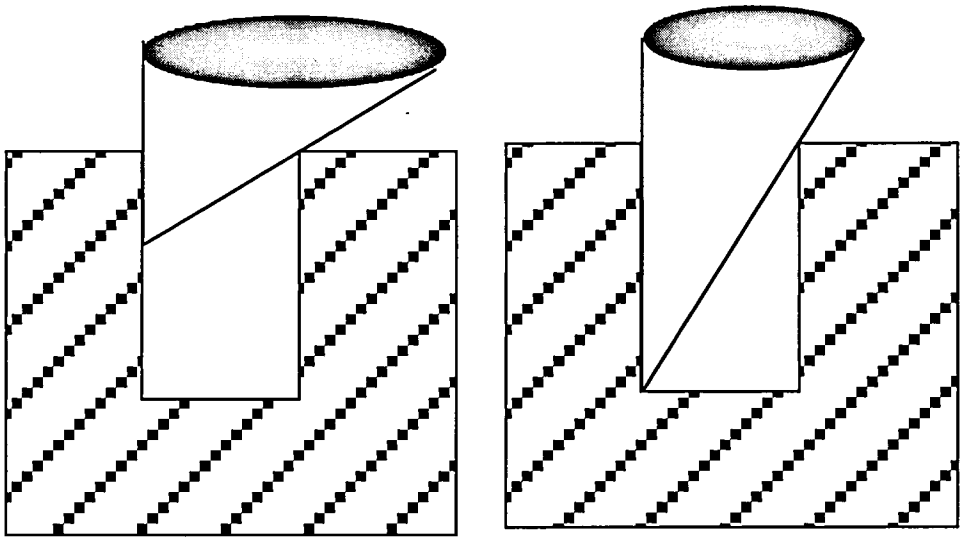
Particle Transport at Low Pressures

Above Wafer --- Mean Free Path << Chamber Dimensions
Viscous Flow --- Gas-gas Collisions

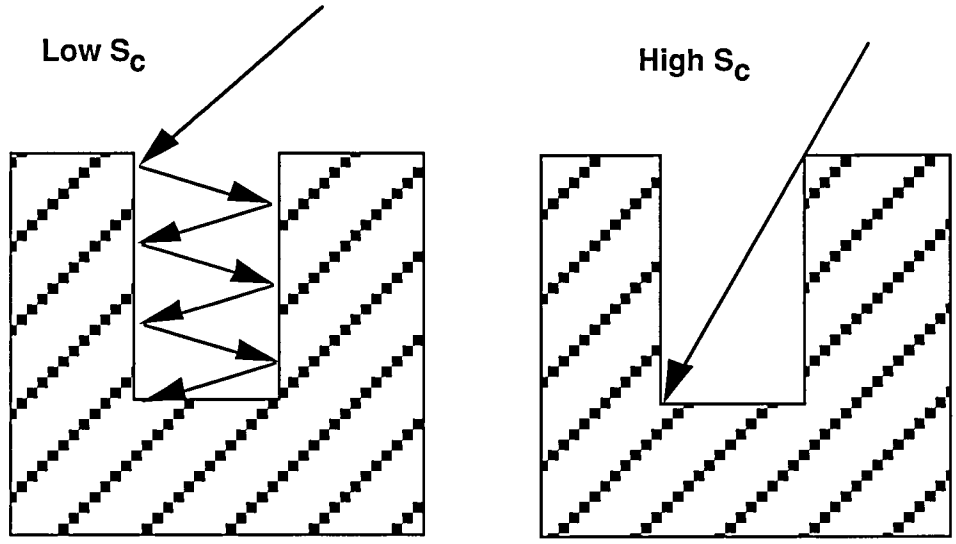
Near Water Surface ... Mean Free Path >> Device Dimensions
Molecular Flow -- Gas - wafer surface collisions

Since the mean free path for LPCVD and PECVD 10 μ m and for sputtering a few cm we can ignore collisions between the gas particles when they are inside a via or a trench like structure. The only collisions are those with the surface of the wafer.

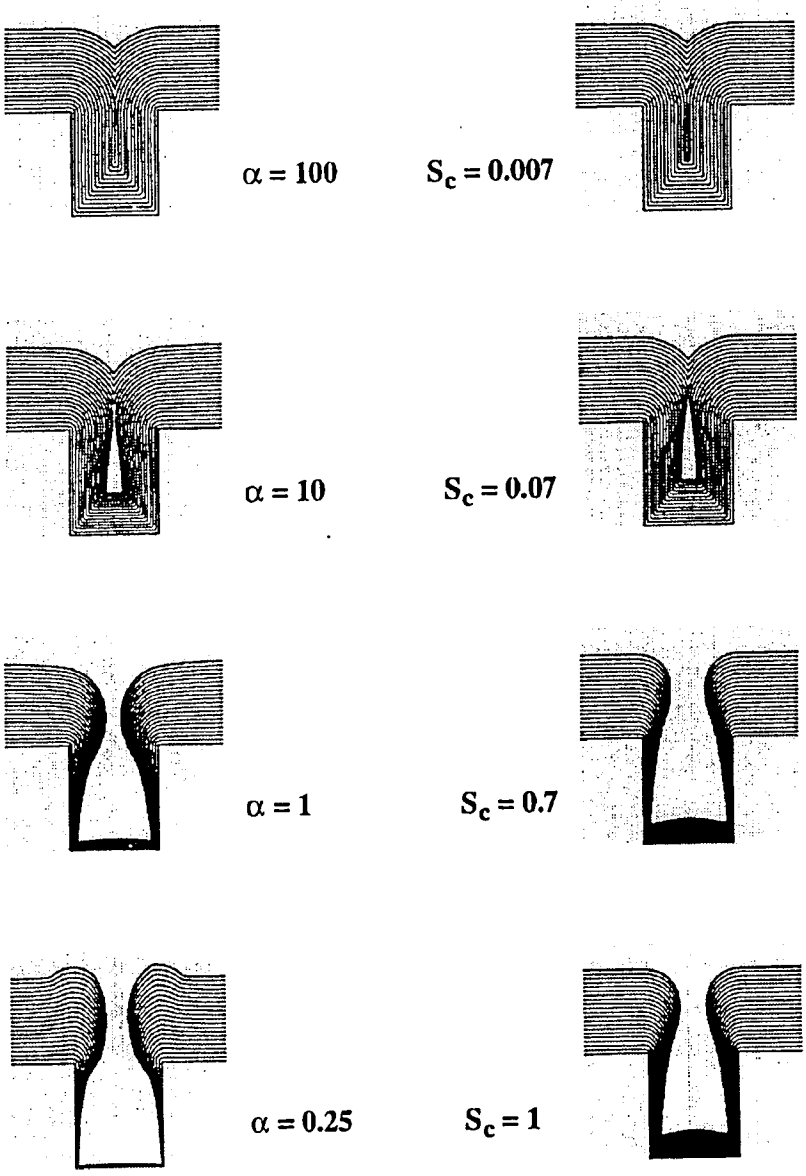
Shadowing of the direct flux by the walls reduces the flux at the bottom corners of a via or a trench resulting in thinner deposition.



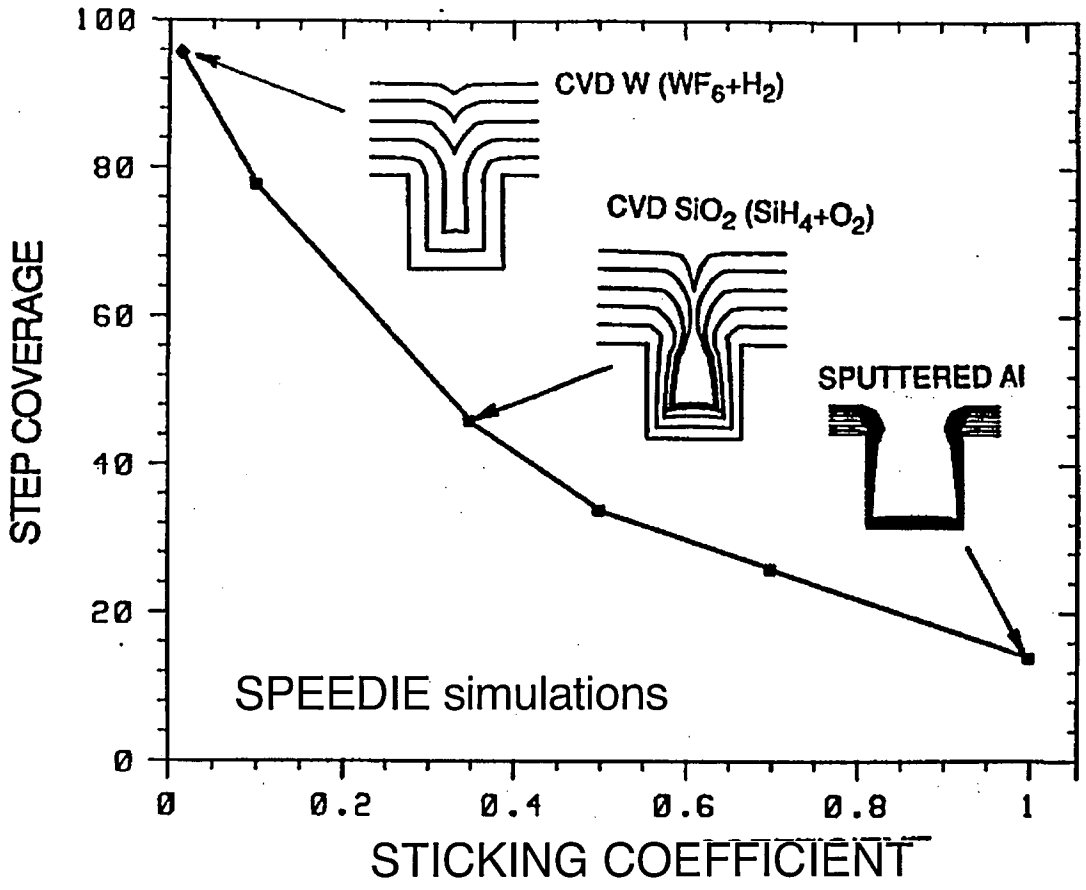
Lower sticking coefficient increases the number of bounces and hence increases the probability of deposition precursors reaching the bottom. Hence, step coverage is better for lower S_C.



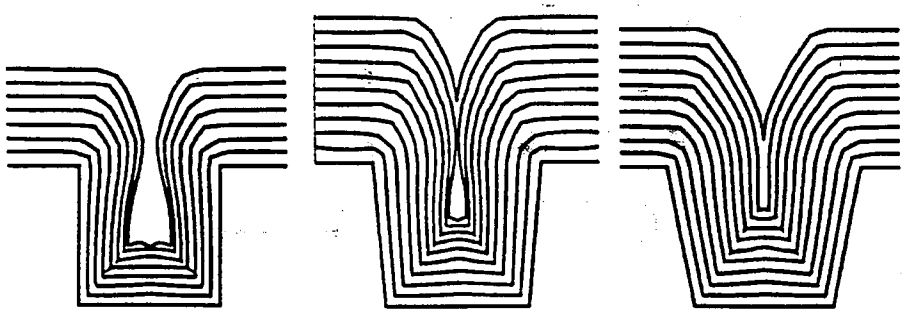
APCVD **LPCVD**



$$\alpha = \frac{D}{KS} = \frac{\textit{Gas phase diffusivity}}{\textit{Surface reactivity} \bullet \textit{Diffusion layer thickness}}$$



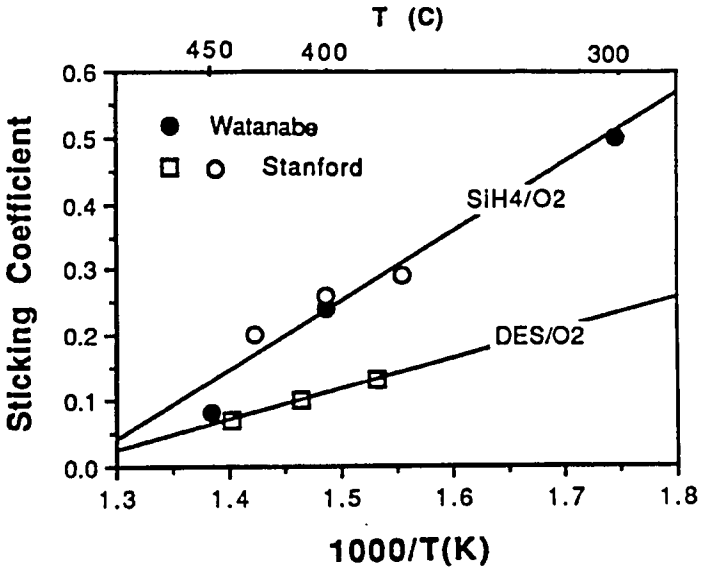
Step coverage can also be improved by changing the slope of the walls. But this may result in an area penalty.



90° 85° 80°

Time evolution of the profile

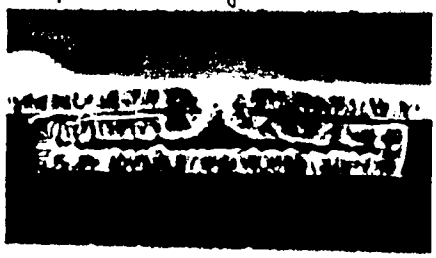
Different lines show time evolution of the profile as simulated by the deposition and etch simulator SPEEDIE

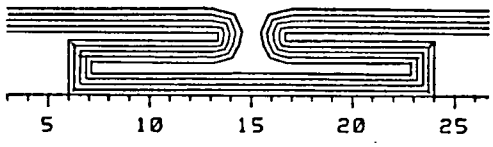


K. Watanabe et al, J. Electrochem. Soc., 137, p1222, 1990

Material	*Source*	*Temperature* °C	S_c
PSG	SiH_4/ O_2/ PH_3	400	0.35
SiO_2	SiH_4/ O_2	400	0.26
SiO_2	DES/ O_2	380	0.1
SiO_2	TMCTS/ O_2	560	0.04
SiO_2	TEOS/ O_2	700	0.04
Poly–Si	SiH_4	620–900	<0.01
W	WF_6/ H_2	350–500	<0.01

PCVD of tungsten in a cavity showing ex step coverage.





Plasma Enhanced Chemical Vapor Deposition

One of the important limitations of LPCVD is that it requires high deposition temperatures, which may be incompatible with the other process steps,e.g., deposition on an aluminum film. In PECVD, the homogenous gas phase reactions are initiated by neutral collisions with the non-equilibrium energetic electrons produced by a rf plasma instead of thermal energy. Thus the deposition precursors can be produced at much lower temperatures by these homogenous reactions. Furthermore, ion bombardment makes the surface more reactive by creating more dangling bonds (active sites) and/or supply instantaneous energy at the surface for the heterogenous reaction to take place. In general, PECVD can be carried out at a much lower temperature than LPCVD. Moreover the deposition rate is found to be higher in PECVD than in LPCVD.

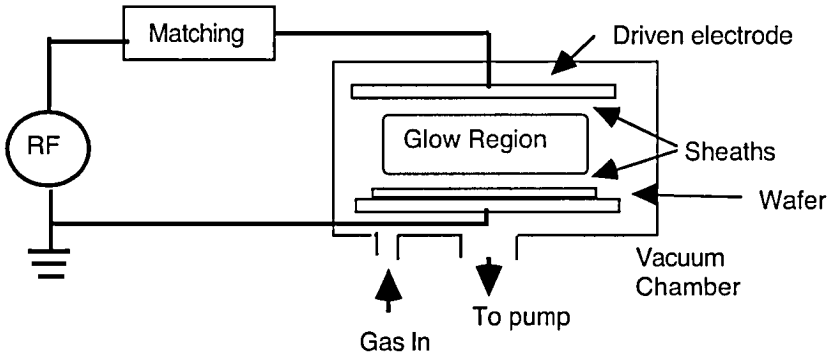


Fig 7. Parallel plate plasma enhanced chemical vapor deposition reactor

There are a number of different reactor configurations used for PECVD but the physical principle is the same in all cases. Figure 7 shows the schematic of a cold wall, parallel plate plasma deposition reactor which is very similar to an etching reactor. The chamber consists of two electrodes, one of which is grounded and the other is powered by a rf source. The wafers are placed on the grounded electrode and are heated from below to the desired temperature by resistive heaters or high-intensity lamps. The reactant gases are introduced at the outer periphery, they flow radially towards the center from where they are pumped out. A plasma is generated between the electrodes by the rf voltage applied across the electrodes. The electrode spacing is about 5 - 10 cm and the operating temperature and pressure are - 400°C and 0.1 - 5 Torr respectively. Homogenous reaction between the reactant gases is initiated by the electrons produced in the plasma. The ions are accelerated towards the electrodes due to the self bias voltage between the plasma and the electrode. These energetic ions bombard the surface, making it more reactive, leading to higher deposition rates.

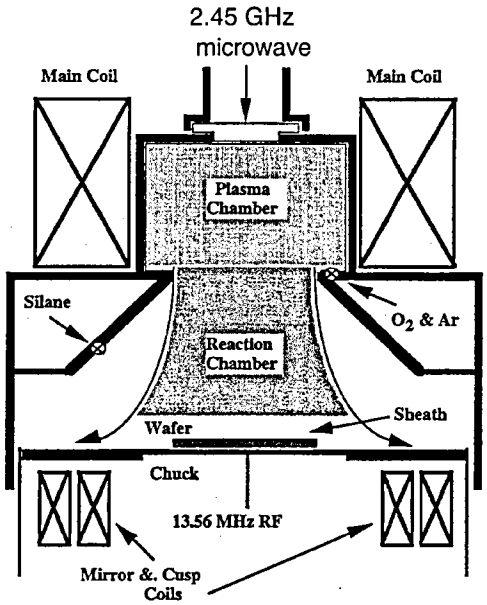


Fig. 8. Electron Cyclotron Resonance (ECR) high density plasma CVD system.

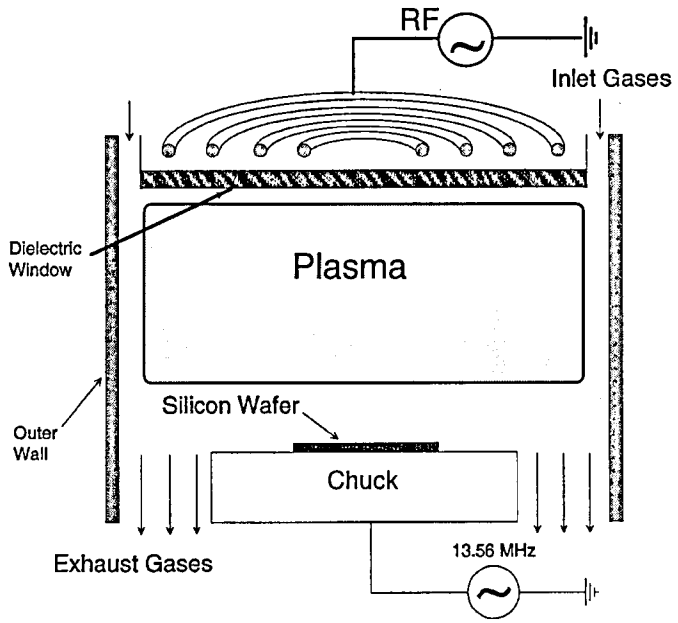
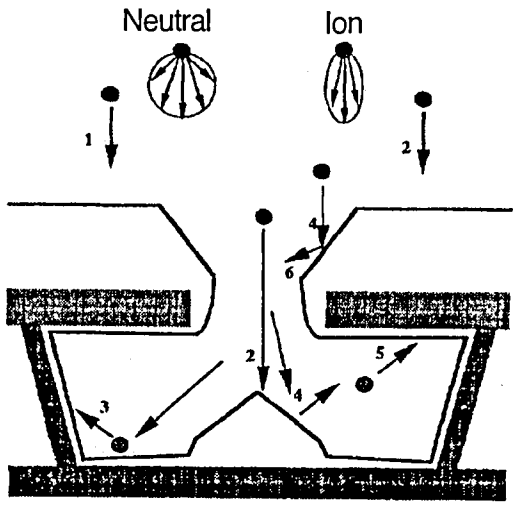


Fig. 9. Inductively coupled high density plasma CVD system.

Fig. 8 and 9 show high density plasma CVD systems. These are very similar to the systems used for etching. Unlike other CVD systems there is no intentional heating. The major difference between the HDP and the parallel plate systems is the independent energy sources for plasma generation and controlling ion energy by biasing the wafer electrode. The high energy ions can sputter etch the wafer. This feature can be used to improve the step coverage to the extent of gap filling in a high aspect ratio gap. The energy imparted by the ions is sufficient to raise its temperature to 300-400°C. Generally the wafers have to be cooled to ensure that the temperature is not too high.

Possible Surface Processes in Ion Induced Deposition

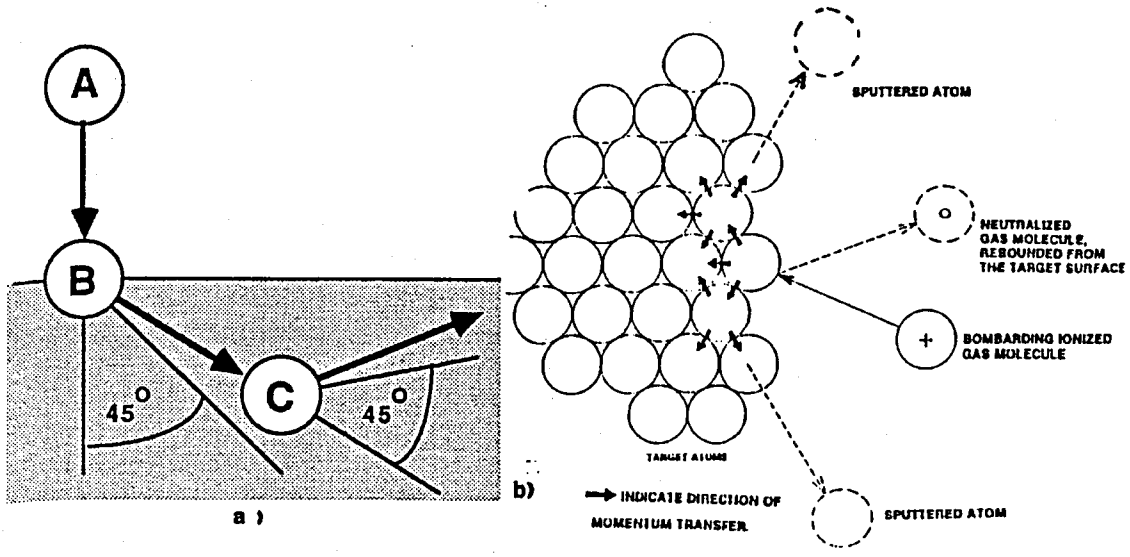
The surface processes can be understood by studing deposition in a cavity like structure with an overhang.



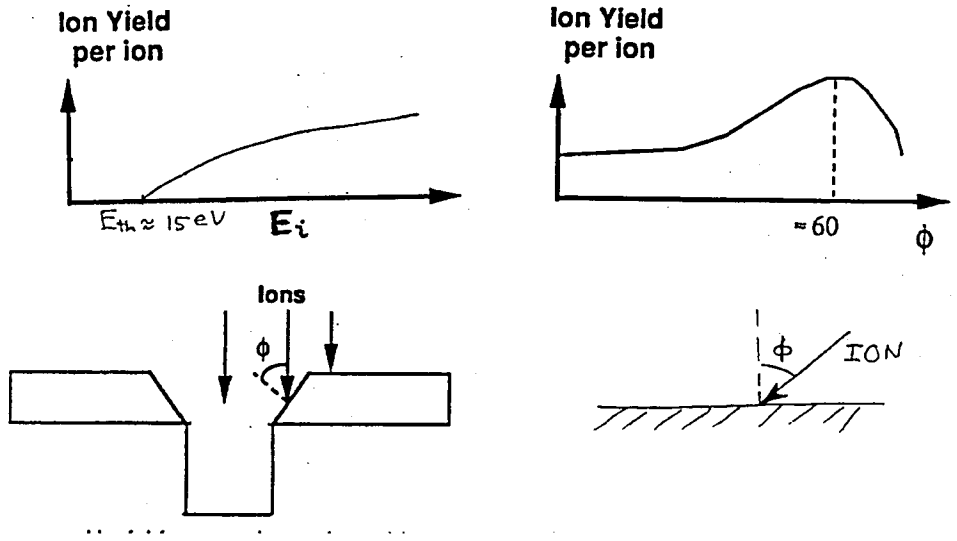
1. Direct deposition from neutral particles
2. Ion-driven direct deposition
3. Indirect diffuse re-emission
4. Resputteriuig of deposited material
5. Redeposition of sputtered material
6. Specular reflection

Sputter Etching Mechanisms

Physical etching involving momentum transfer
--"Atomic Sandbasting"

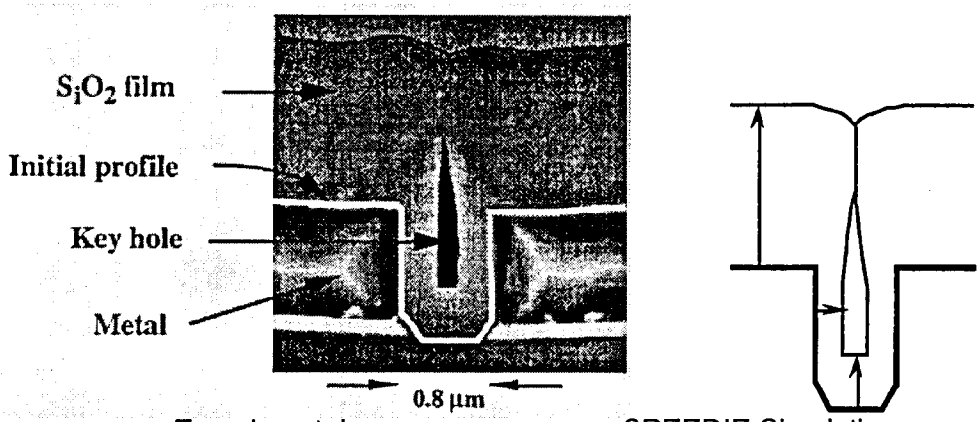


- **Energy and angle dependent**



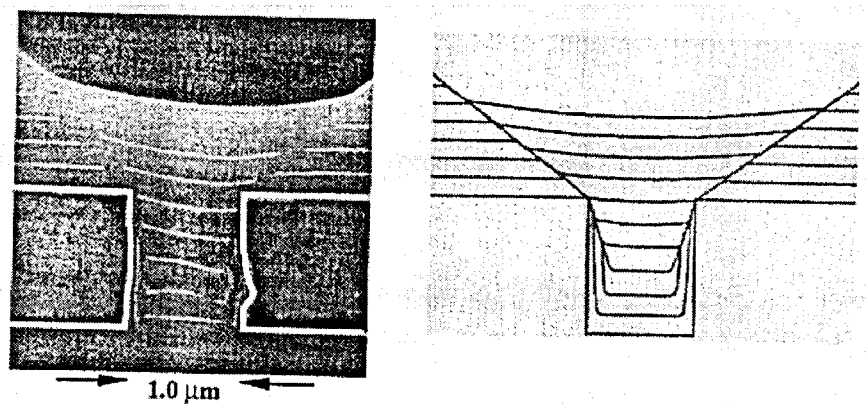
Deposition profile in parallel plate plasma CVD

Only direct deposition from neutral particles and ion-driven direct deposition take place. The deposition rate on side walls is much less than at the bottom, resulting in a key hole like void formation.



Experimental SPEEDIE Simulation

Deposition profile in high density plasma CVD



Experimental SPEEDIE Simulation

In HDP there are energetic ions because of the bias resulting in both deposition and sputter-etching taking place. The relative rates of each process depend upon the ion flux, angular distribution and ion energy.

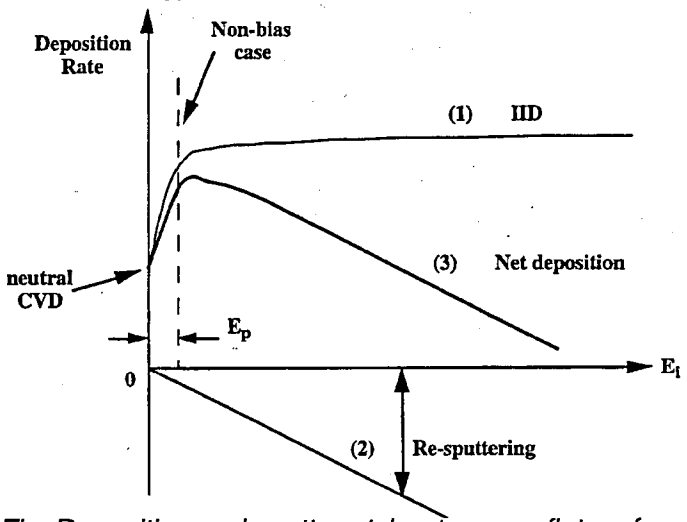
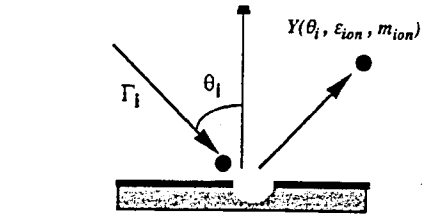
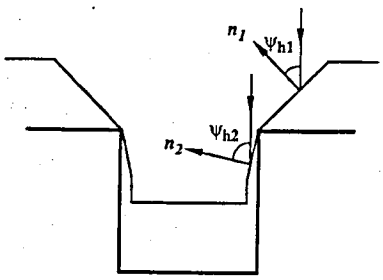


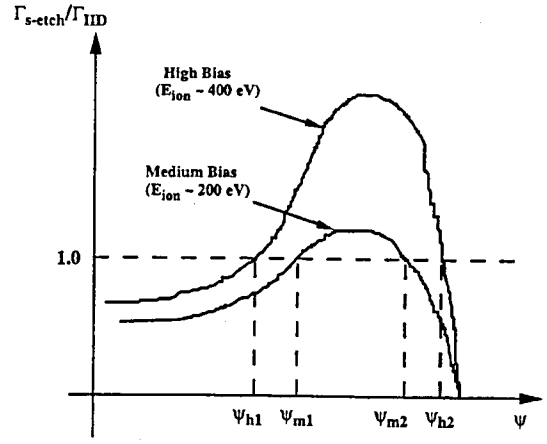
Fig. Deposition and sputter-etch rates on a flat surface

Facet formation due to sputter yield in HDP due to the bias applied to the wafer resulting in energetic ions hitting the surface.





Via or trench



By controlling the facet formation and deposition rates the void formation can be avoided even in high aspect ratio structures.

Physical Vapor Deposition (PVD)

Mostly used for metal deposition

1. Evaporation
   - Filament
   - Electron gun
2. Sputtering

Evaporation

The source of condensable reactive species in physical vapor deposition is either by evaporation or sputtering. In PVD by evaporation, heat is applied to the source of film material causing its evaporation. The evaporated particles get transported to the wafer surface where they condense to deposit the required film. Evaporation is carried out under high vacuum conditions (~ 5×10^{-7} Torr). There are various methods used for the evaporation of the source metals such as resistive heating, electron beam and inductive heating. In resistively heated sources, small strips of the source metal are put on a wire of low vapor pressure metal (e.g. W) which is resistively heated. In electron beam evaporation, a stream of high kinetic energy (5 - 30 key) electrons is directed at the material to be evaporated. The kinetic energy of the electrons is transformed into thermal energy upon impact and supplies the heat required to evaporate the target material. In inductive heating evaporation, the energy for evaporation is supplied by an rf induction heating coil

surrounding the crucible containing the evaporation source. The mean free path of the evaporated molecules during PVD by evaporation is much larger (~ 100 m) than the reactor dimensions, as such the transport of these molecules in the reactor is collisionless ,i.e., is in line of sight.

Though PVD by evaporation has a good deposition rate (e.g. 0.5 μmlmin. for Al) and low surface damage and impurity incorporation, it has some important limitations:

i) Accurately controlled alloy compositions are difficult to obtain.
ii) Filament life is very short.
iii) Film uniformity across the wafer and the step coverage is not as good as sputter deposition.
iv) There may be x-ray damage to the film if an E-beam source is used.
v) High melting point materials, e.g., tungsten cannot be as easily deposited by evaporation (especially by filament) as by sputtering.
vi) In-situ cleaning of the substrate surfaces is not possible.

Sputtering

Because of the limitations of the evaporation process, sputtering deposition is the most widely used PVD technique. Moreover, sputter deposition offers a better control of the process such as film thickness, and film properties such as grain size and step coverage. In sputter deposition highly energetic ion beams are directed against a target to dislodge (sputter) the target molecules, which are subsequently transported to the wafer surface where they condense to form the desired film. Sputter deposition is performed at moderately low pressures (2 - 100 mtorr) in an inert gas (generally argon) ambient. In reactive sputter deposition, the reactor is filled with a reactive gas which reacts with the sputtered material and deposits compound films, e.g. TiN. The energetic ions used to strike the target materials to be sputtered are generated by glow discharges.

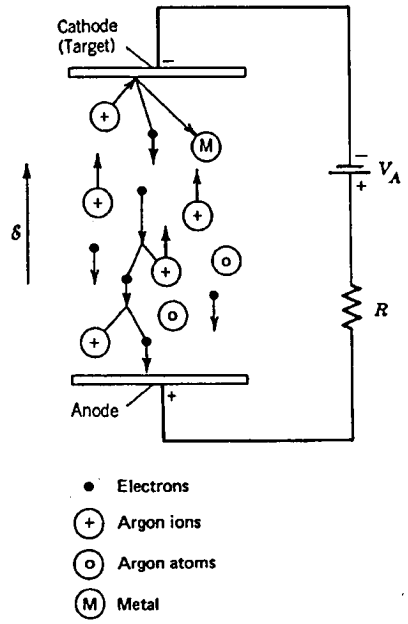


Fig. 10. A dc sputtering system

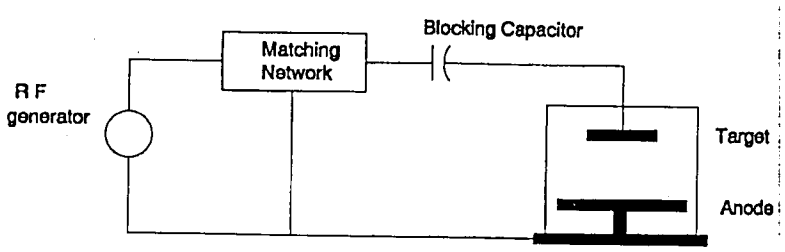


Fig.11: An rf sputtering system

The commonly used techniques for sputtering the target material are:

i) radio frequency (rf) sputtering and
ii) magnetron sputtering (rf or dc).

In a rf sputtering system, positive ions are generated by collisions of neutral species with the electrons in the plasma, which is sustained by a rf current. The ions gain energy by being accelerated towards the target due to the voltage across the plasma sheath. Today most PVD is done by sputtering using a magnetron. For conductors a dc source is usually used, while for insulators an rf source is used. Magnetron sputtering increases the electron utilization by confining the electrons, which cause ionizing collisions, near the target surface with the help of magnetic fields. Current densities achieved in magnetron sputtering systems are much higher (10 - 100 mAlcm2) compared to rf sputtering sources (1 mAlcm2). The figure below shows a schematic diagram of a planar magnetron target. In planar magnetrons, the target surface is planar and the magnetic field is created by magnets behind the target. It is seen from this figure that half way between the magnet poles, the magnetic field (B) lines are parallel to the target face and since the electric field (E) is perpendicular to the target face, the E x B field closes on itself in this region, establishing a continuous path for the trapped "hopping" electrons. Therefore, the plasma density is highest in this region of maximum E x B resulting in very rapid sputtering. This region is called the "race track". The powersupplies in magnetron sputtering may be dc or rf. DC power supplies can be built to supply up to 20 kW, whereas rf power supplies are limited to - 3 kW. Therefore, dc magnetron sputtering can provide higher deposition rates than rf magnetron sputtering, and consequently is more widely used. The distance between the target and the wafer is typically 5 - 10 cm, the operating pressure is - 2 - 10 mtorr and the elecctrode voltage is a few hundred volts. In most cases the wafer is kept at normal room temperature, however, some times heating is also used.

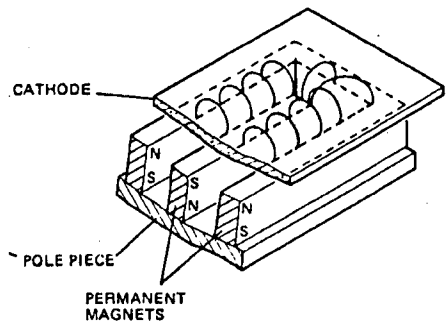
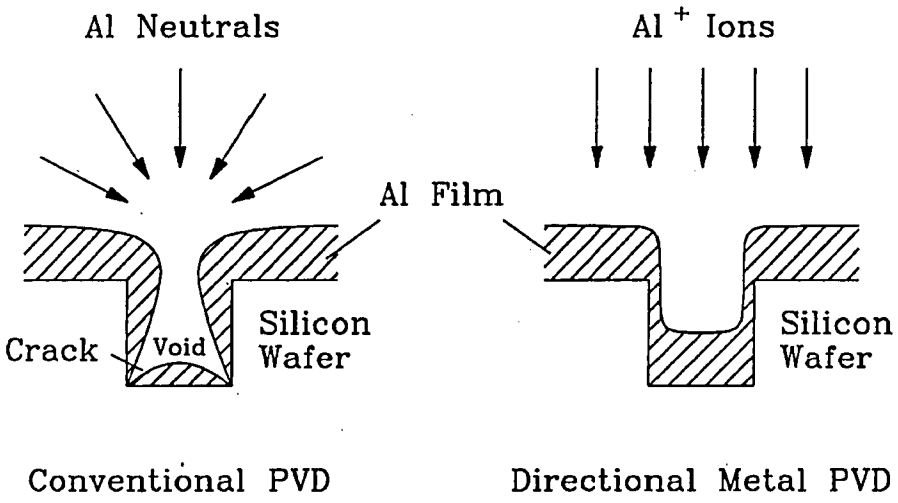


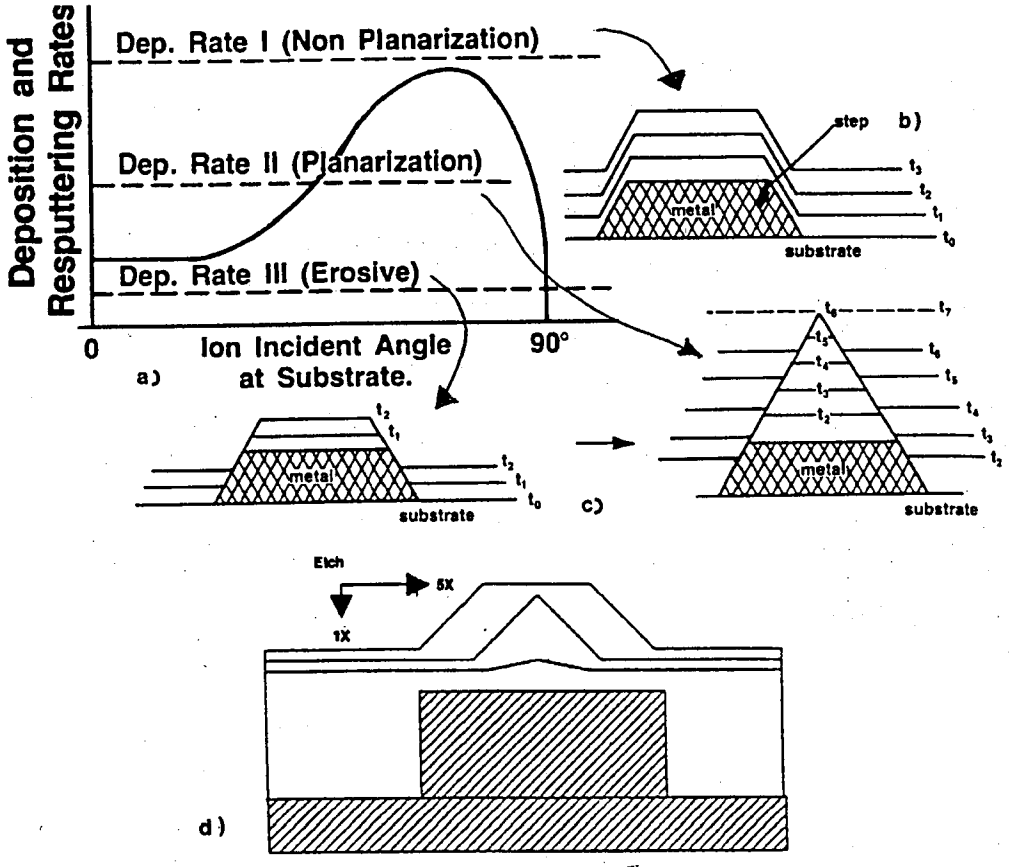
Fig. 12 Schematic diagrams of a planar magnetron target.

Deposition profile in Sputtering



The step coverage can be improved by increasing the surface diffusivity by heating the wafer during or after the deposition.

Bias Sputtering



Degree of planarization

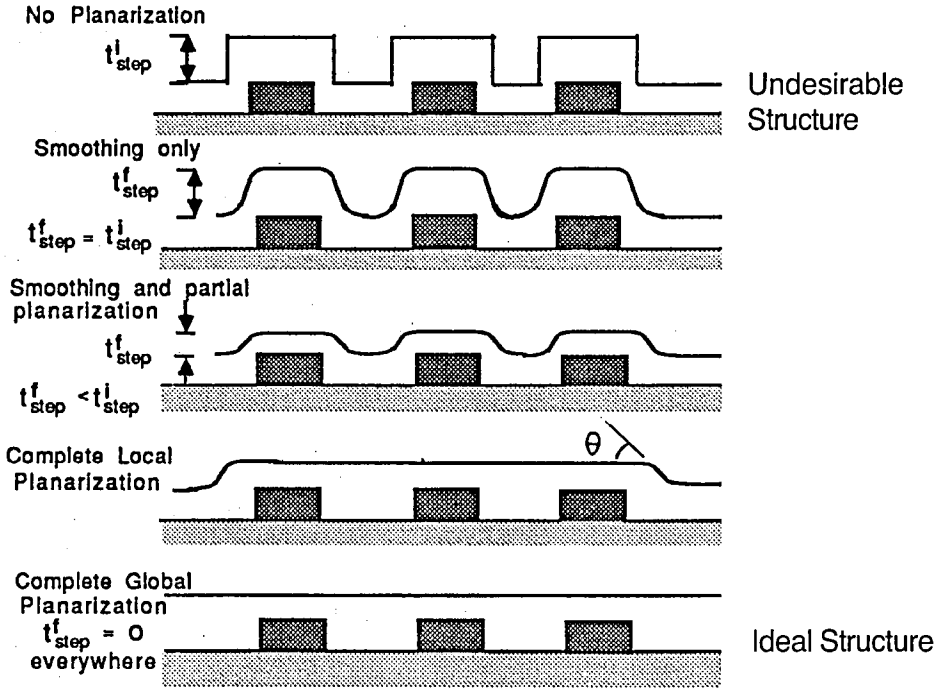


Fig. 4. Degree of Planarization.

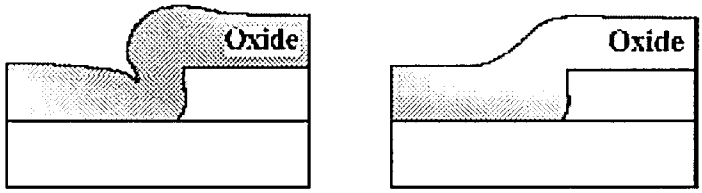
$$\text{Degree of Planarization} = 1 - \frac{t^i_{step}}{t^f_{step}} \qquad \text{slope} = \theta$$

Planarization Methods

- Reflow of SiO_2 doped with phosphorus and boron glass
- Reflow of metal
- LPCVD of tungsten
- Etch-back of a sacrificial layer
- Simultaneous etch and deposition
- Organic spin coating
- Chemical Mechanical Polishing (CMP)

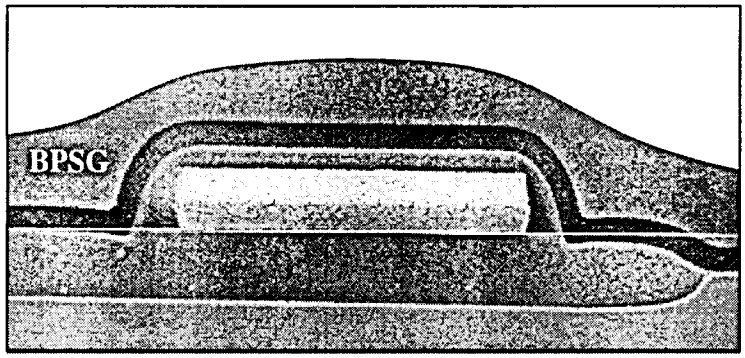
Reflow of Doped SiO_2 (First level dielectric)

Addition of B_2O_3 and P_2O_5 concurrently further decreases the viscosity. Viscous flow is a strong function of the ambient.

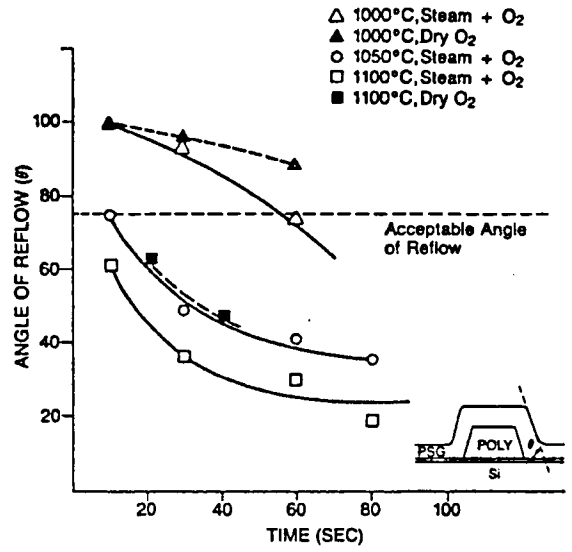


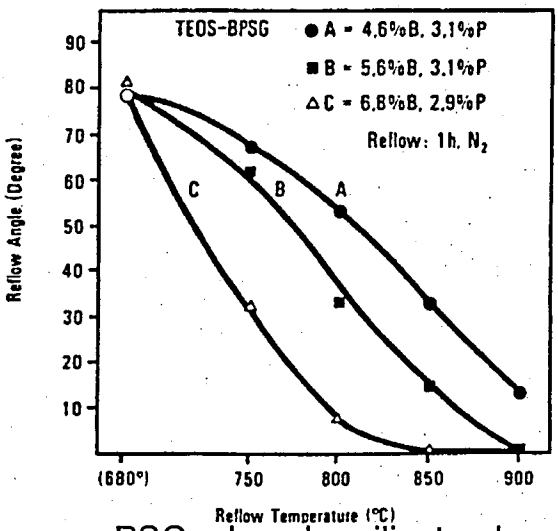
a b

Figures above show topography of silane-based LPCVD oxide layer over a step: a. as-deposited, or annealed with no dopant in oxide; b. after anneal with dopants like phosphorus and boron in oxide, showing reflow.



Above is SEM image of BPSG oxide layer after 800°C reflow step, showing smooth topography over step.

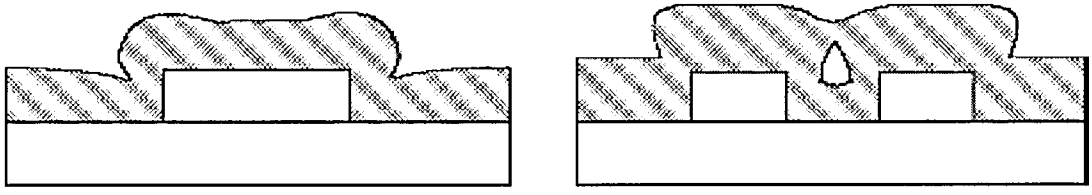




- PSG: phospho-silicate glass, will reflow at 950 - 1100°C
- BPSG: boro-phospho-silicate glass, will reflow at 800°C.

Intermetal dielectric are also made of SiO_2, but cannot be subjected to reflow or densification anneals.

• Two common problems occur cusping and voids.



a b

Etchback Planarization Using Sacrificial Layers

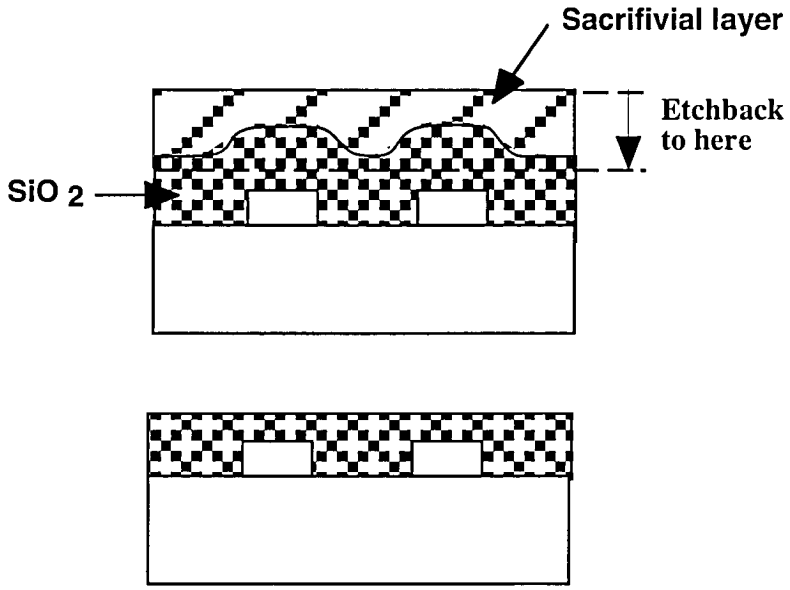
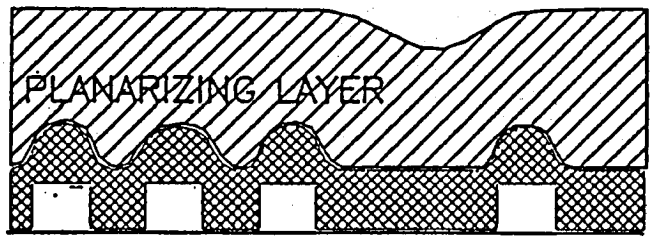


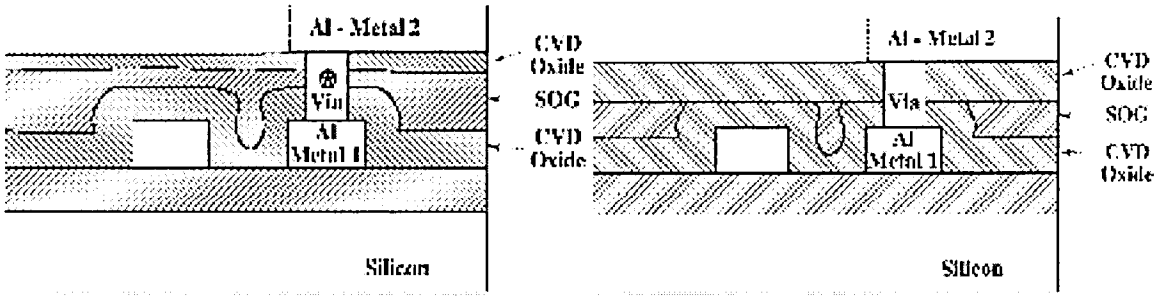
Illustration of photoresist etchback process. Photoresist is deposited over rough topography, then the structure is etchedback, leaving a smooth top surface of the oxide.



More realistic profile due to micro loading resulting in local planarization.

Spin-on-glass (SOG)

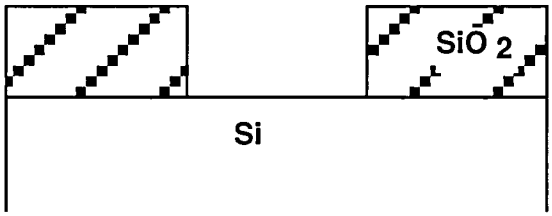
- Fills like liquid photoresist, but becomes SiO_2 after bake and cure.
- Done with or without etchback (with etchback to prevent poisoned via).
- Can also use low-K SOD's. (spin-on-dielectrics)

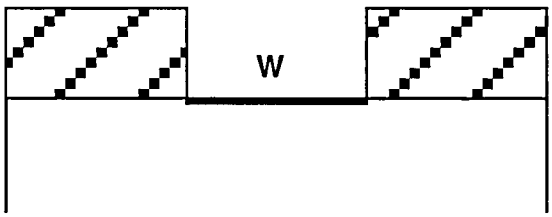


without etchback **with etchback**

- SOG oxides not as good quality as thermal or CVD oxides
- Use sandwich layers.

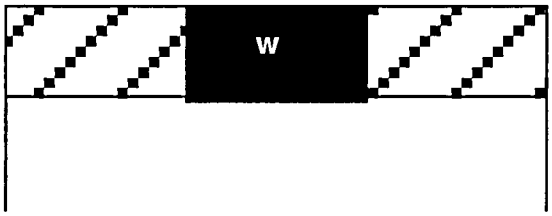
Selective CVD of W





$2WF_6 + 3Si = 2W + 3SiF_4$

Deposition only on Si
Limiting thickness



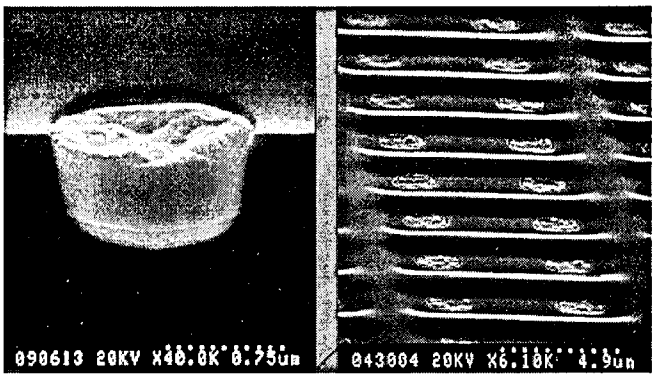
$WF_6 + 3H_2 = W + 6HF$

Deposition only on W

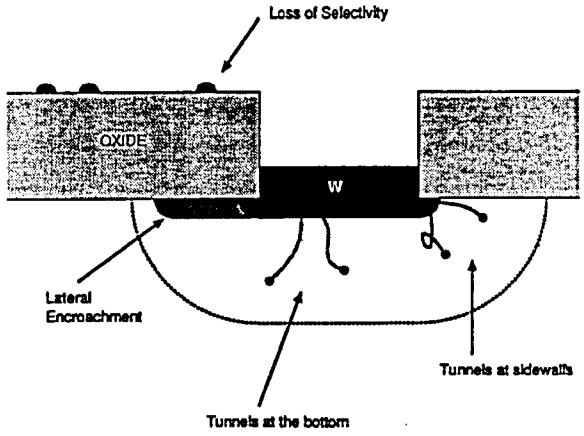
For the hydrogen reduction to occur atomic hydrogen is needed

$$H_2 <-> 2H$$
$$WF_6 + H -> W + HF$$

The dissociation of H_2 to H occurs readily on metallic surfaces, but not on dielectric surfaces. Hence the overall deposition is selective.



This technique has been demonstrated for filling vias and many other applications, e.g., strapping of poly-Si and source drain junctions similar to the salicide technology. However, there are many problems which have impeded the acceptance of this technology in manufacturing.



Problems of Selective CVD of W

- Loss of selectivity
- Lateral Encroachment
- Tunnels

The last two problems take place during the initial deposition of W. during the Si reaction with WF_6 any crystal imperfection enhances the reaction. Generally heavily doped regions always have some defects. Loss of selectivity results because of contaminants and dangling bonds.

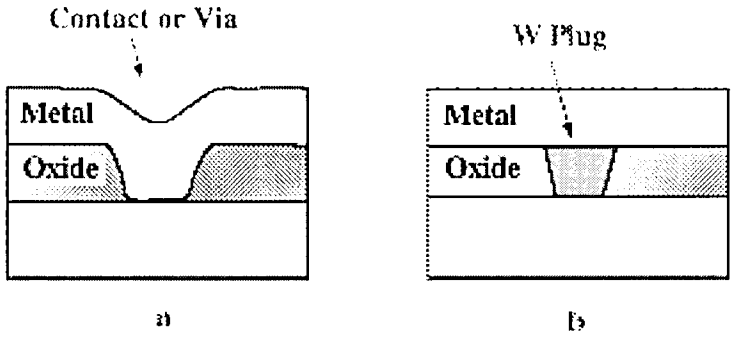
Non-Selective CVD of W

Tungsten can also be deposited by SiH_4 reduction of WF_6, however, the deposition is non selective.

$$WF_6 + SiH_4 \rightarrow W + HF + SiF_4$$

HF and SiF_4 are gaseous byproducts.

• A commonly used planarization technique is the use of W plugs for contacts and vias:



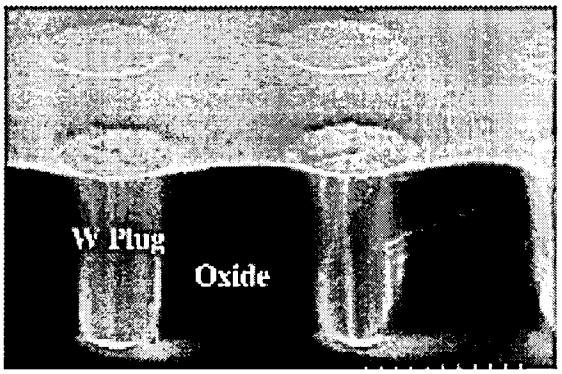
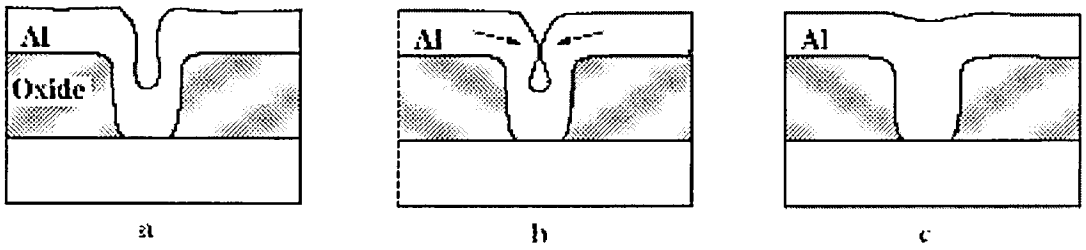


Fig. SEM image of W plugs after blanket CVD deposition and CMP. Photo courtesy of VLSI Technology, Inc.

Generally adhesion of CVD W to SiO_2 is poor. Therefore, a glue layer is used as an adhesion promotor. The best choice is TiN.

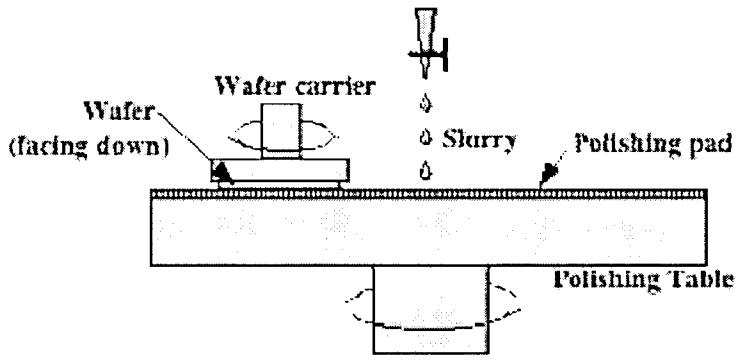
Reflow of Metal

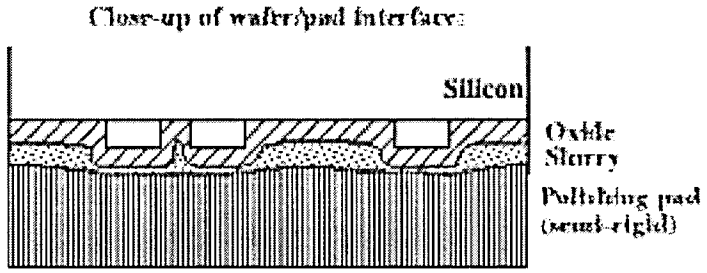
A planarization method that does involve Al as a contact or via material is reflow.

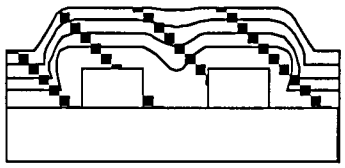


Wafer is heated at 450-550°C to help fill contact or via and planarize structure. Driving force for reflow is surface energy reduction.

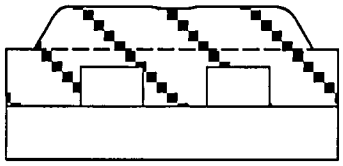
Chemical-Mechanical Polishing (CMP)







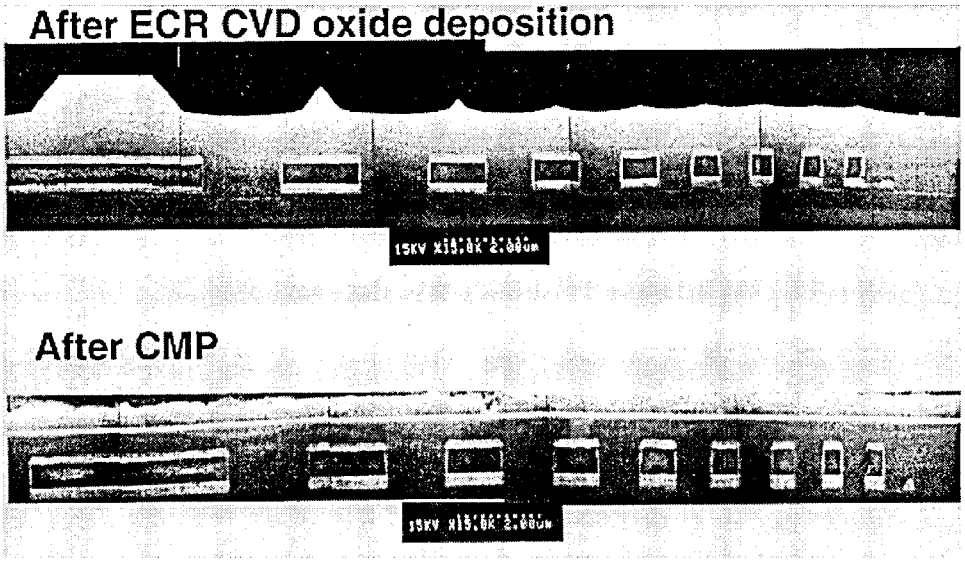
1. deposit thick oxide



2. etch off top

3. globally planarized topography remains

- CMP, once considered a technique too crude and dirty for IC fabrication, is now commonly used.
- Global, or near global, planarization can be achieved.
- Can be used for dielectrics, as well as for metals (W plug, for example).



Air gaps lower k of interconnect dielectrics

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Ben Shieh, Krishna Saraswat, Mike Deal, Jim McVittie, Stanford University, Stanford, California

Established CVD oxide processes can be fine-tuned toproduce air gaps between metal lines to lower the k of interconnect dielectric stacks. Design constraints and integration challenges exist, but air gaps may be easier to integrate than completely new low-k materials. Manufacturable processes can reduce interconnect capacitance by as much as 40-50% for tightly spaced metal lines.

As IC technology scales, the performance of ULSI chips is increasingly limited by the capacitance of the currently used intermetal dielectric: SiO2 [1]. The capacitance of the interconnect dielectric influences the chip speed (RC delay), AC power (CV2f), and crosstalk. A great deal of development is being done on new materials and fabrication technologies to reduce the interconnect capacitance. Current low-k dielectrics under investigation include fluorinated SiO2, amorphous carbon-fluoride, aerogels, and polymers. Using air or vacuum as the only dielectric has also been explored [2].

Unfortunately, the new low-k materials under investigation pose many challenges of reliability, manufacturability, and integration. Some of these issues include: 1) mechanical strength, 2) dimensional stability, 3) thermal stability, 4) ease of pattern and etch, 5) thermal conductivity, 6) CMP compatibility, and 7) complexity of integration. Most low-k materials currently being researched are inferior to SiO2 in most if not all of the above properties [3].

Additionally, as ICs continue to scale, the aspect ratio of metal lines increases so that the intralevel dielectric (IaLD) capacitance increasingly dominates the interlevel dielectric (IeLD) capacitance in determining total interconnect performance (Fig. 1). Thus it becomes increasingly important to implement low-k schemes between tightly spaced metal lines and less so between metal levels [3].

Air gaps formed between metal lines during SiO2 deposition address many of the concerns associated with low-k materials while offering comparable if not better capacitance reduction [4-7]. Air gaps reduce the dominating IaLD capacitance, while leaving the IeLD SiO2 intact to maintain the structural integrity of the interconnect stack. Additionally, since no new materials are introduced, new etch and CMP recipes are not needed and thermal stability is not an issue. Air gaps do, however, present a number of integration and reliability issues that must be addressed before introduction to manufacturing.

Electrical performance

Capacitance simulations. We used a rectangular "box" air-gap geometry to simulate how capacitance reduction varies with air-gap dimensions [4]; the metal height was 0.7 ?m and the IeLD thickness was 0.9 ?m. A relative dielectric constant of 4.1 (typical of deposited SiO2) was used for both the IaLD and IeLD material. The effective dielectric constant, keff, was calculated by dividing the simulated capacitance of the total geometry by the simulated capacitance of the metal geometry in vacuum (k = 1). The calculated keff values are comparable to, or better than, most of the homogeneous low-k materials currently being investigated.

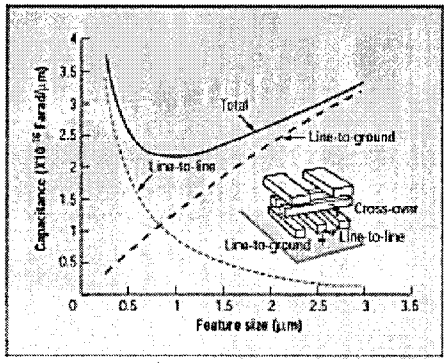


Figure 1. As IC technology scales, the aspect ratio of metal lines increases so that the intralevel line-to-line capacitance increasingly dominates the interlevel capacitance [3].

SST/Feb/Shieh/Fig 1

Although the "box" may not be a realistic air-gap shape, simulations using this shape can assist in determining the important air-gap dimensions affecting capacitance. Simulations become particularly important when deciding how to tailor the air-gap shape to balance the tradeoffs between capacitance reduction and reliability.

Modeling of air-gap technology can be extended from the simple box capacitance models to simulating the deposition used to form air gaps in real-world structures. We simulated a typical air-gap profile with SPEEDIE (Stanford Profile Emulator for Etching and Deposition in IC Engineering). This profile can then be input to an electrical simulator to model the capacitance.

Simulations can predict the capacitance of arbitrarily spaced lines. For example, after obtaining experimental data for the IaLD air-gap structural capacitance between 0.3 and 0.4 ?m spaced lines, SPEEDIE can simulate the deposition and extrapolate what the capacitance might be on wider-spaced lines.

Experimental results. Figure 2 shows a SEM image of air-gap structures processed in a collaboration between Texas Instruments and Stanford University [4]. The air gaps shown were fabricated in a 0.3/0.3-?m line/space array using an HDP-CVD process. Figure 3a shows the electrical data measured on single level metal comb structures with air gaps fabricated using this process. The electrical data for comb structures with HDP-CVD SiO2 gap-filling the space between metal lines is also shown for comparison. Assuming the gap-fill oxide has a relative k of 4.1, the median keff for the air-gap structures is approximately 2.47, a 40% reduction in capacitance.

Figure 3a also demonstrates the uniformity of the process. As the cumulative probability plot shows, the distribution of the air-gap capacitance data is similar to - if not better than - the distribution of the HDP-CVD oxide gap-fill capacitance data. Additionally, there is no significant difference in current leakage data between the air gap and HDP-CVD oxide samples.

Figure 4a shows a SEM image of air-gap structures fabricated at Matsushita [5]. In this process, an over-etch into the oxide layer extends the air gaps below the metal lines, and ensures that no oxide is deposited between the metal lines. As the box simulations predict, extending the air gap above and below the metal lines can be quite effective in reducing capacitance. The capacitance data for these air-gap structures is shown in Fig. 4b.

Process integration and reliability

Unlike most low-k interconnect schemes currently being researched, the use of air gaps does not introduce any new or exotic materials to the process flow. Consequently, no new etch or CMP recipes are required, and process temperatures do not need to be reduced (as is the case for relatively thermally unstable polymers). Air-gap integration issues center on physical compromise of the air gap during subsequent processing, such as in CMP and via formation.

If air gaps extend significantly above the metal lines, then they may be opened during subsequent CMP. Even if the CMP does not remove enough SiO2 to reach an air gap directly, the normal and shear forces during CMP may create enough stress to compromise the interconnect structure.

To ensure that the air gap is not opened during subsequent processing requires that the deposition process be engineered to control the extent of the void above the metal lines. When engineering the process, it is important to consider the deposition topography within and above varying line spaces. A problem with nonconformal depositions is that, while an air gap may form nicely between tightly spaced lines, an air gap formed between wider-spaced lines during the same deposition will be positioned significantly higher relative to the metal lines. There is also the possibility of forming a low quality "seam" that continues through the deposition even after the air gap has pinched off.

One process flow developed at Sandia National Labs solves the problem of forming air gaps in the varying spaces between intralevel metal lines without requiring an additional masking step [6]. The SiO2 deposition is stopped after air gaps are formed between the smallest spaces. A low-k spin-on dielectric (SOD) then fills the re-entrant features in wider spacings that have not yet pinched off. An oxide deposition finally caps the SOD to provide a uniform material surface for CMP. The disadvantage of this process is that it introduces a low-k spin-on material that must be etched through during via definition.

The air-gaps fabricated at Matsushita (Fig. 4a) were shaped by a two-step process (Fig. 5) [5]. A conventional PECVD SiO2 process forms the initial air gap. Then, an HDP-CVD gap-fill process prevents air gaps in the wider metal spacings from extending too far above the metal lines. The HDP-CVD step fills the wider spacings between metal lines, but the sealed off air gaps in the smaller spacings remain.

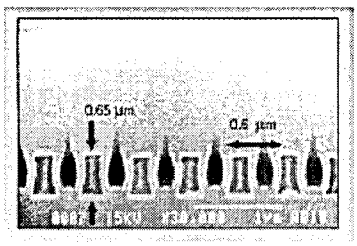


Figure 2. SEM of air-gap structures in an array of 0.3-?m lines and spaces. The "I-beaming" of the metal lines is an artifact of the cleave.

True metal profiles exhibit only a slight taper.

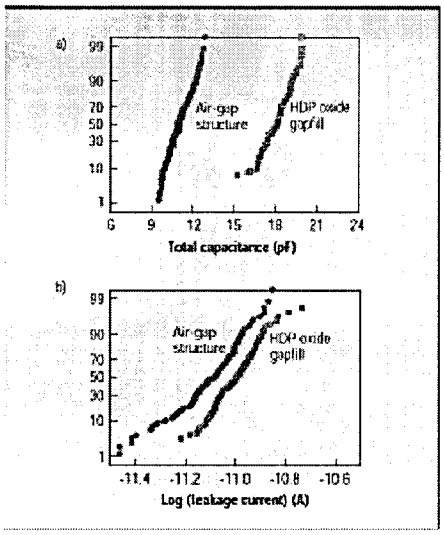


Figure 3. Electrical data for comb structures with air gaps fabricated at Texas Instruments. Air-gap split a) shows 40% reduction in capacitance, and b) does not show appreciable leakage [4].

SST/Feb/Sheih/Fig. 3

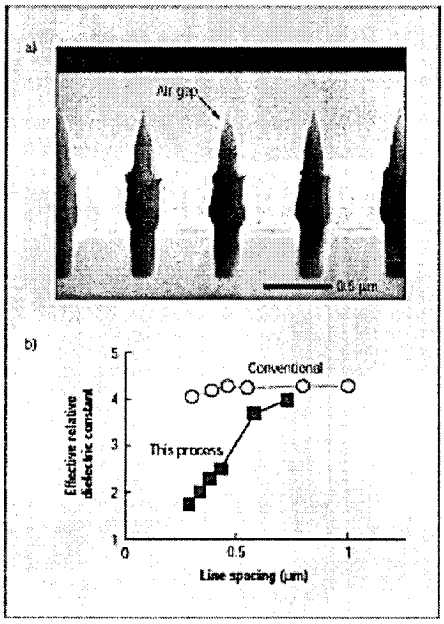
We used a similar two-step approach to fabricate the air-gap structures in the Texas Instruments/Stanford work. However, instead of using a PECVD process in a conventional chamber, we developed a PECVD-like process (high gas flow and low substrate bias) for a HDP-CVD chamber to form the air gaps. After some time to allow the air gaps to form, the gas flows to the chamber were decreased and the substrate bias increased, switching to an HDP-CVD gap-fill process that fills the wider spaces. The high sputter component of the second step also prevents a seam from forming above the smaller spaces. This process improves throughput and allows the use of a single process chamber instead of two. In all three of the processes discussed, the experimental air gaps fabricated withstood subsequent CMP.

Another process integration concern is that a slight misalignment during via lithography may result in the air gap`s opening during via etch. Again, control of the air-gap shape and size may be critical to address this issue, especially as technology moves toward zero overlap vias. The process developed at Matsushita gets around this problem by fabricating the vias before the air gap (Fig. 5). In this process, vias are formed above the unpatterned blanket metal layer. Once the vias are formed, the SiO2 ILD and metal are etched using the same mask step. The SiO2 deposition to form the air gaps then follows.

A future concern for air-gap structures is that of integration with metal damascene processes. This will become an important issue with the move from aluminum to copper wiring. With damascene metal processes, integration of air gaps becomes slightly more complicated but can be accomplished without additional masking steps. A process for incorporating air-gap structures with damascene metal is being developed at Stanford; the details will be presented in future publications.

Thermal reliability. Because air or vacuum has such poorthermal conductivity, one must assess the thermal performance of interconnect stacks incorporating air gaps. Increased temperatures in the interconnect stack due to Joule heating can result in many reliability problems, including enhanced electromigration.

The table on page 57 summarizes the simulation results of a five-metal-layer interconnect geometry with different dielectric configurations [7]. The simulation geometry consisted of arrays of aluminum metal lines at each level with a pitch of 0.72 ?m. Each metal layer was 0.8-?m thick, and each IeLD layer was1.0-?m thick. For all simulations, a current density of 0.5 mA/cm2 was used in simulating Joule heating. The silicon substrate at the bottom of the stack was assumed to be the only heat sink in the system. As the table shows, the temperature rise in the air-gap interconnect system is only minimally higher than the homogeneous SiO2 case. In contrast, the interconnects utilizing homogeneous low-k materials may exhibit prohibitively high temperature rises.



SST:Feb/Sheih/Fig. 4

Figure 4. Air-gap structures fabricated at Matsushita: a) SEM, and b) electrical data [5].

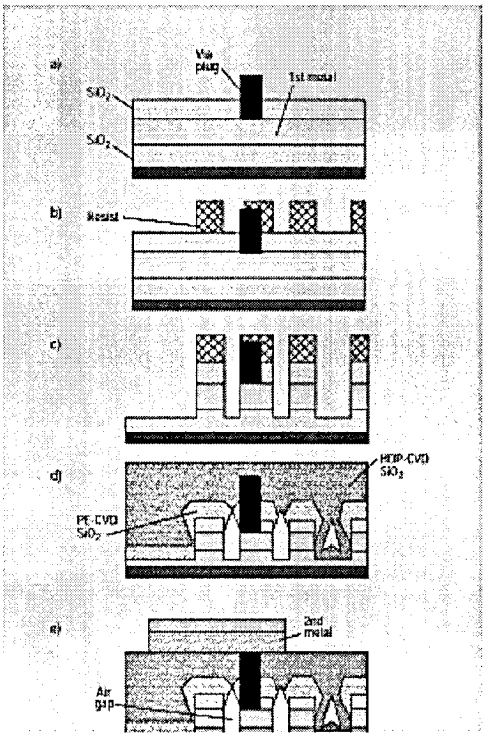


Figure 5. Process flow for Matsushita-made air gaps [5]; a) via plug formation; b) resist patterning of first interconnect; c) first interconnect formation; d) intermetal dielectric deposition; e) second interconnect formation.

SST/Feb/Shchl/Fig. 5

The results can be modeled by a thermal resistance circuit. In each metal layer, the vertical thermal conductivity is dominated by the metal leads and not by the intralevel dielectric between them - whether it be SiO2, low-k material, or vacuum. Between metal layers, however, the thermal conductivity is limited by the IeLD material. In the case of air gaps, the IeLD material is still SiO2, which has a thermal conductivity an order of magnitude higher than typical polymers. It has been shown that the presence of vias does not significantly help heat conduction through the IeLD layers [8].

Temperature rise above substrate temperature in five-metal-layer interconnect stacks

	Current through all metal leads	Current only through top metal leads
Homogeneous SiO_2	4.9 K	1.9 K
Homogeneous low-k material	76.7 K	28.0 K
Air gaps w/ SiO_2 IeLD	5.2 K	2.0 K

Electromigration reliability. Another concern with the use of air gaps in interconnect structures is that there may be increased likelihood of metal extrusions, because the sidewall SiO2 passivation is very thin on closely spaced interconnects. To address this concern, the interconnect group at Stanford developed a modeling strategy to assess the tradeoffs between reliability and performance in interconnects using air gaps [9]. In these simulations, SPEEDIE simulated the formation of air gaps of varying sizes. The air-gap profiles were then input to MARC (a finite element model) to simulate electromigration-induced stress arising from increasing volumetric strain in the aluminum lines. Contour plots were then generated of the maximum principal stress for structures with different air-gap sizes.

In this model, the failure mode studied was SiO2 sidewall cracking at some critical value of the tensile maximum principal stress, acrit(SiO2). Following the methods of Knowlton et al., an approximate MTTF for each air-gap case can be deduced from the critical acrit(Al) required to induce failure [9].

Preliminary experimental electromigration data for two air-gap splits fabricated at Texas Instruments were compared with hydrogen silsequioxane (HSQ) embedded low-k SOD and HDP-CVD SiO2 gap-fill [7]. Data were collected for open failures after 1.75 mA/cm2 at 250?C applied stress. Contrary to the initial modeling results, the lifetime of the air-gap samples - even with a thin sidewall thickness (<100 nm) - were statistically the same as the HDP-CVD SiO2 and the HSQ. Although data for the shorting has not yet been obtained, one would normally expect that cracking of the oxide sidewall and subsequent extrusions would reduce the electromigration back-stress, resulting in faster open failures.

Conclusion

Air gaps can reduce interconnect capacitance by as much as 40-50% for tightly spaced metal lines. This capacitance reduction is comparable to or better than that obtained by most low-k materials currently under investigation. At the same time, the use of air gaps addresses many of the integration and reliability concerns associated with currently investigated low-k materials. Air gaps do present a number of integration and reliability issues of their own, and additional work is needed before this technology can be introduced to manufacturing. However, the work done thus far on air-gap integration shows promising results.

Acknowledgments

The authors would like to thank Somnath Nag, R. Scott List, and Robert Havemann of the Semiconductor Process and Development Center at Texas Instruments for their support. We would also like to acknowledge Tetsuya Ueda of the ULSI Technology Development Center at Matsushita Electronics Corp. and James Fleming of Sandia National Labs for their cooperation in providing original figures from their papers on air-gap technology.

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